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MS-7B28

ATX:234mm\*185mm

Intel -CoffeeLake-S plamform

CPU:

LGA1151

CPU POWER PAK \*4Phase

GT POWER PAK \*2 Phase

System Chipset:

H310

Onboard Chip:

SIO: NUVOTON 5567

HD Audio Codec: ALC887

LAN: INTEL I219V

Flash ROM: SPI 64 MB

CUT VBAT:SLG4B41231

PWM:

VCORE - RT3607138A

VGT- RT360745A

DDR - RT823111.525A

DDR VPP25- MP21431.12A

PCH(1.05V) - RT8125E10.743A

VCCSA - RT8125E11.1A

VCCIO - SY82886.4A

Main Memory:

DDR4 \* 2 (Dual Channel)

ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:GS7133+N MOS

1P8\_VSB:GS7166

3VDSW:L11831

VCCSTPLL:GS7133

Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1 ) Slot \* 2

MSI

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Size Custom

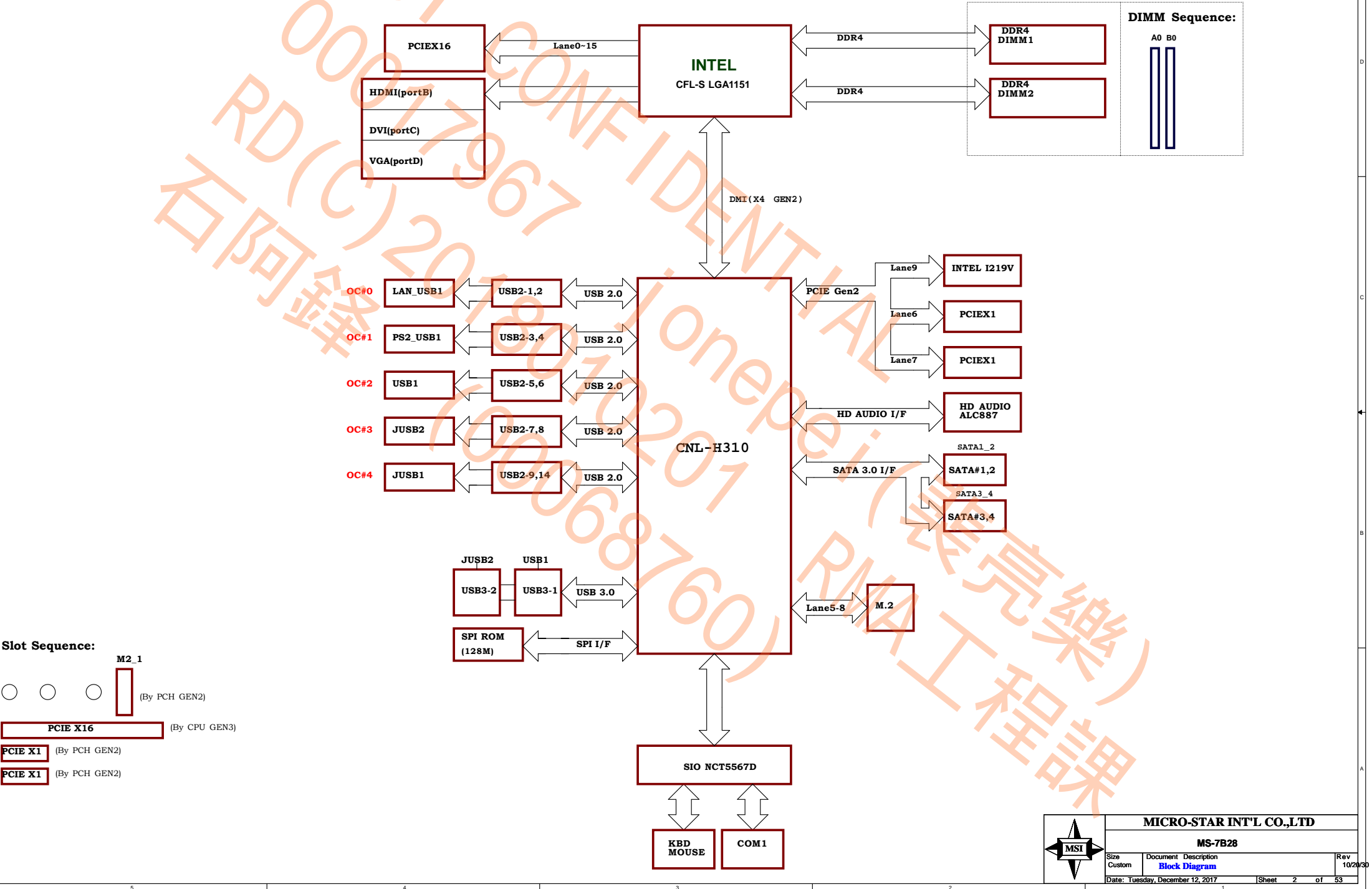
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Rev 10/20/30

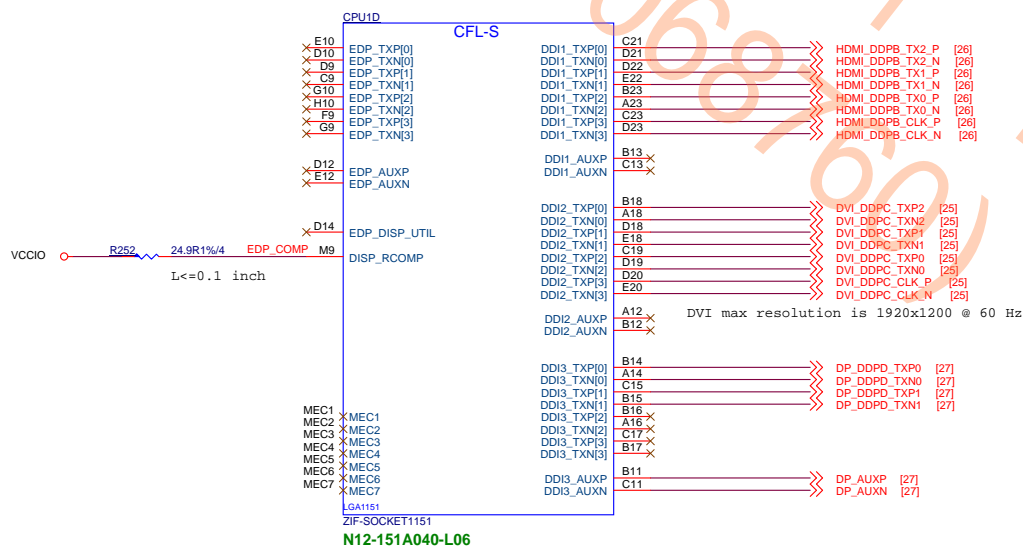
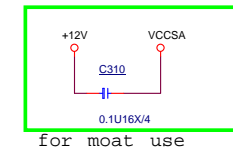
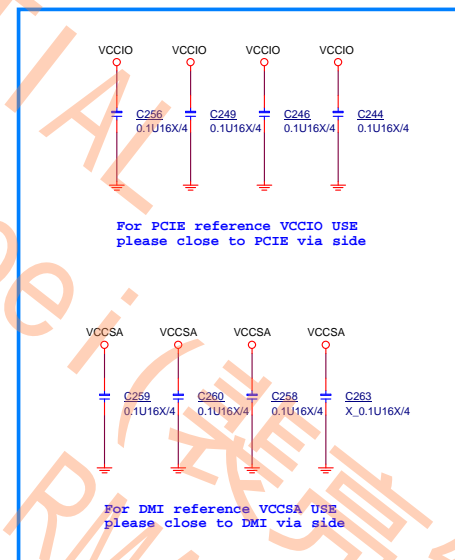
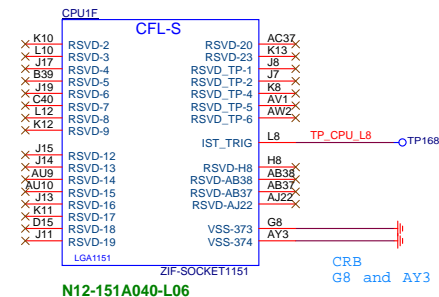
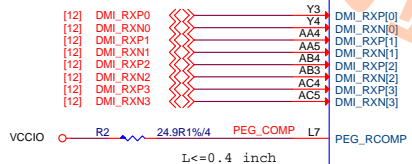
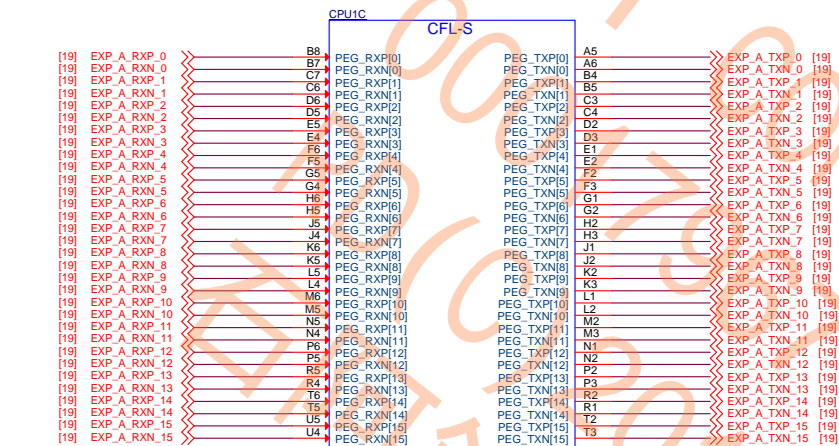
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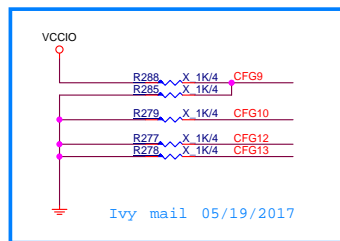
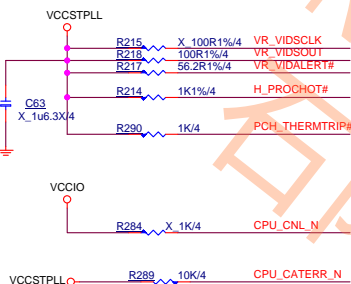
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Block Diagram

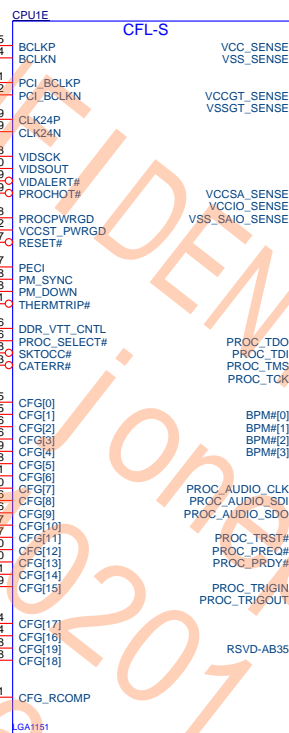
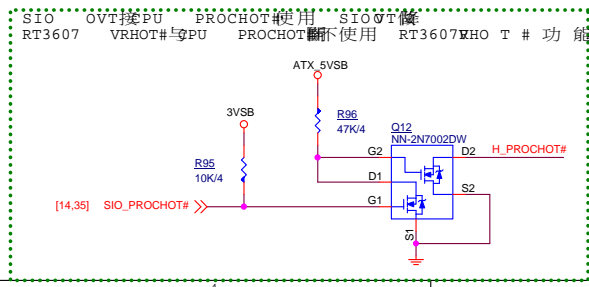




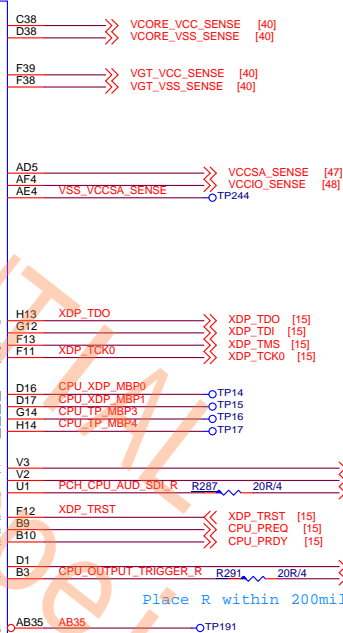




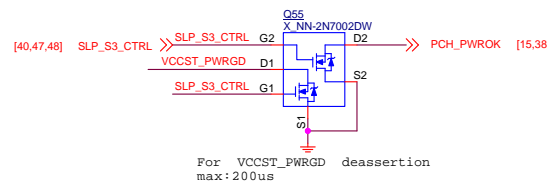
CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL Lock
1			RSVD
2	NORM	REVERSE	REQ_LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PGOCFGSEL[0]
6	DISABLE	ENABLE	PGOCFGSEL[1]
7	RESET#	BIOS REQ	REQ_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		RSVD
15	RSVD		RSVD



N12-151A040-L06



POWER DOWN-板拿掉

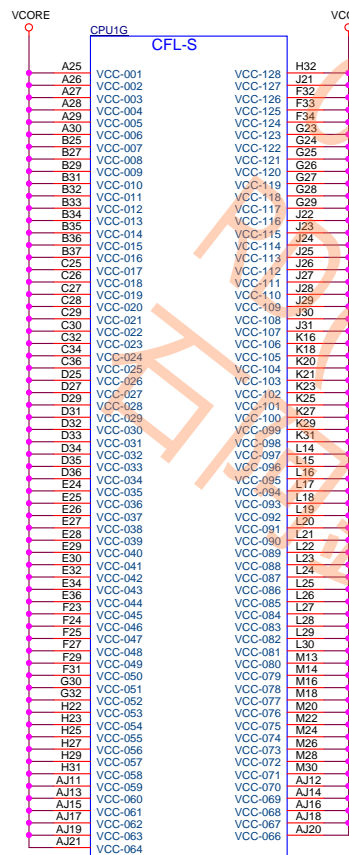


For VCCST\_PWRGD deassertion max: 200us

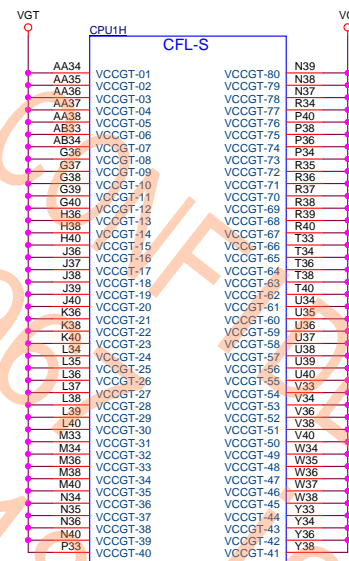


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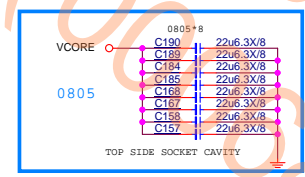




LGA1151  
ZIF-SOCKET1151  
**N12-151A040-L06**

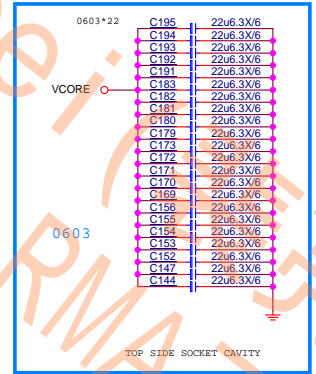


LGA1151  
ZIF-SOCKET1151  
**N12-151A040-L06**



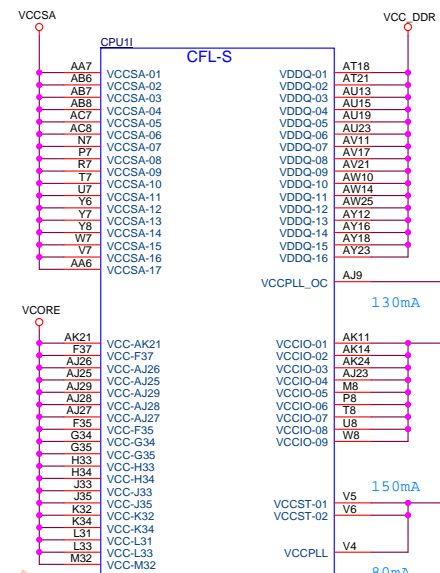
0805

TOP SIDE SOCKET CAVITY

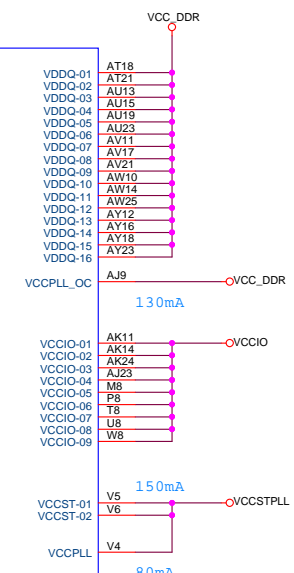


0603

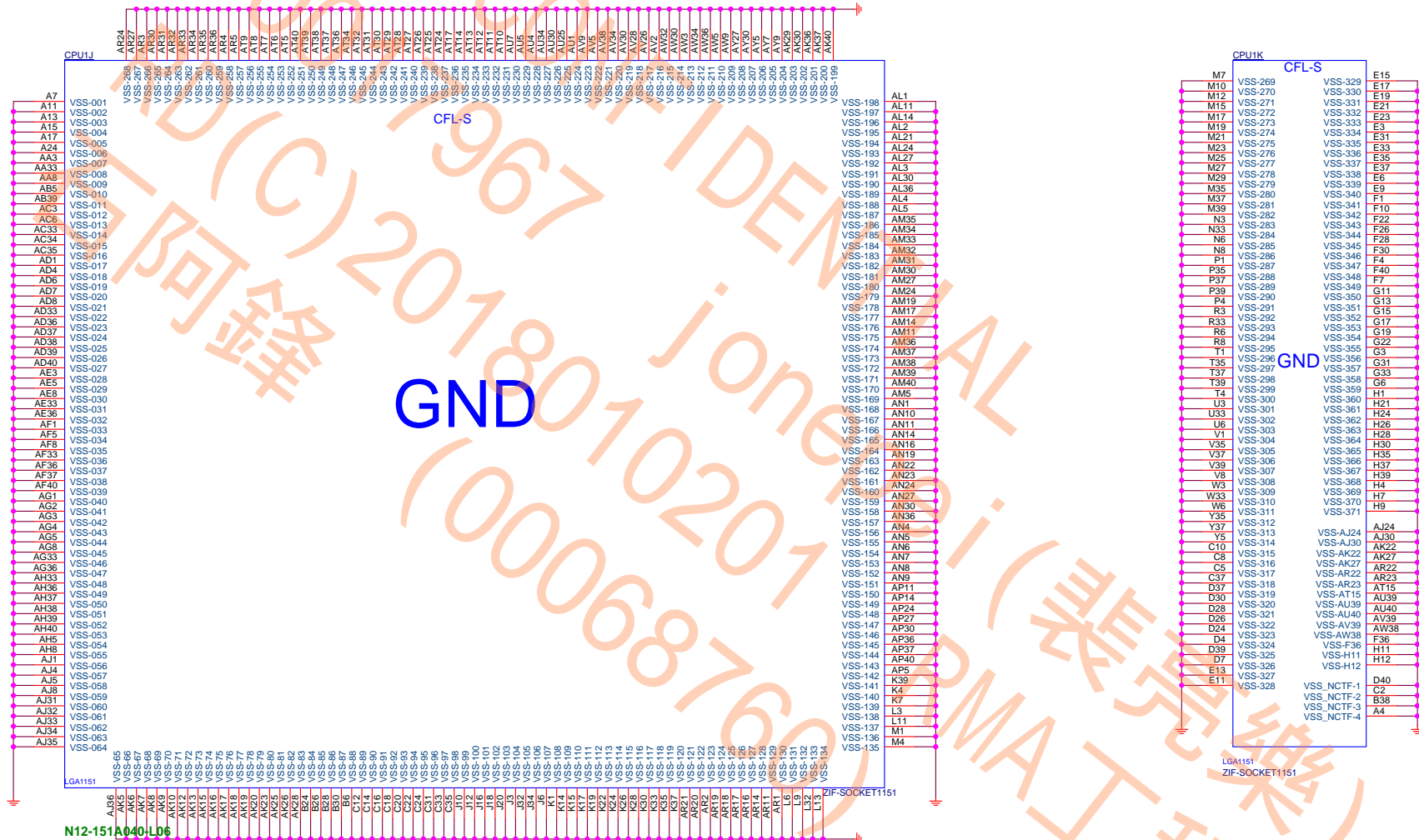
TOP SIDE SOCKET CAVITY

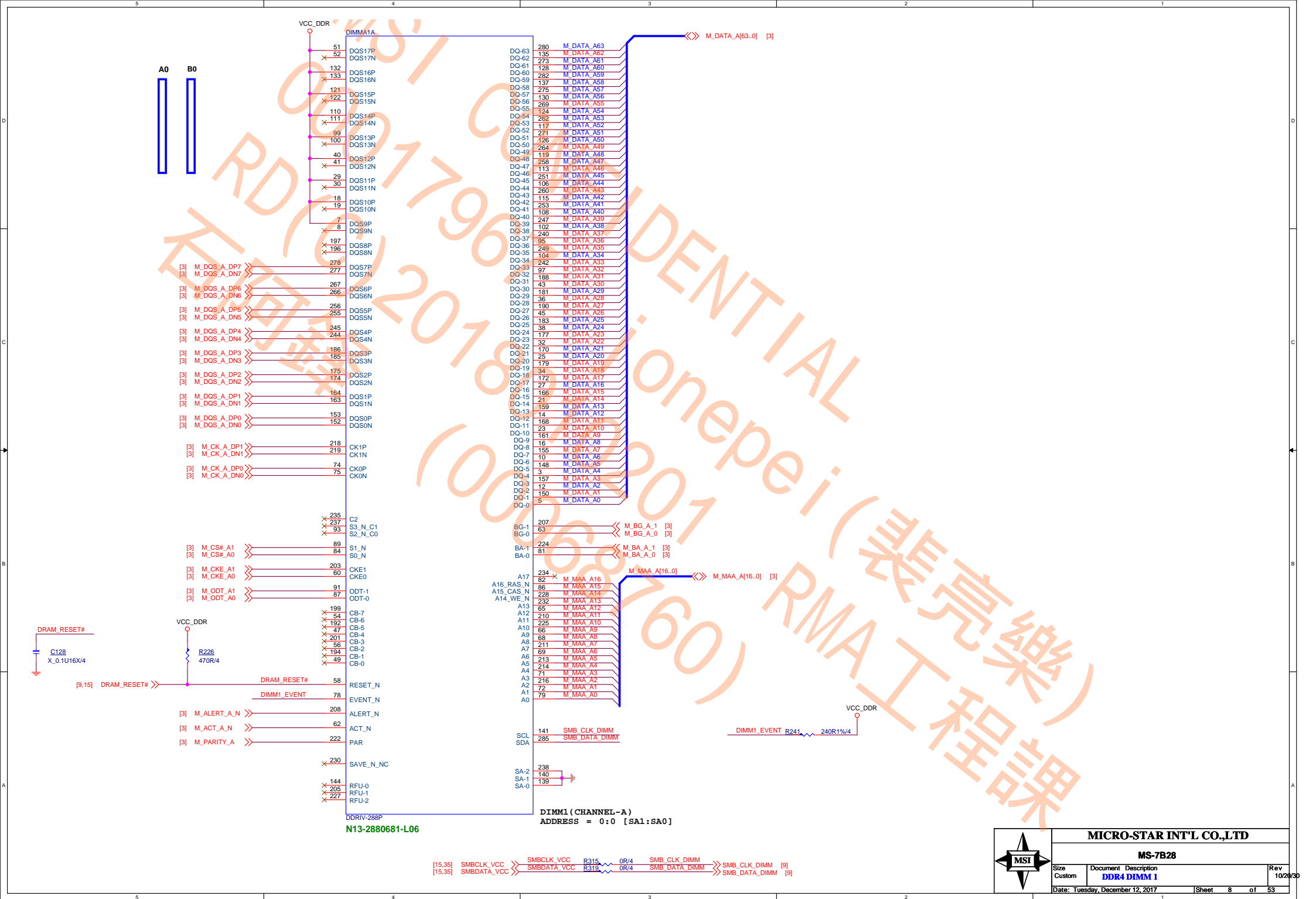


LGA1151  
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**N12-151A040-L06**

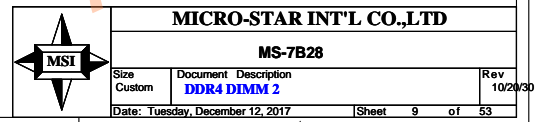


MICRO-STAR INT'L CO.,LTD			
MS-7B28			
Size	Document	Description	Rev
Custom		CPU-Power	10/20/30
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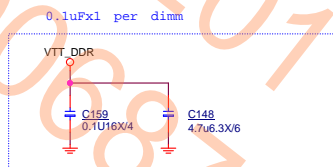
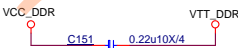
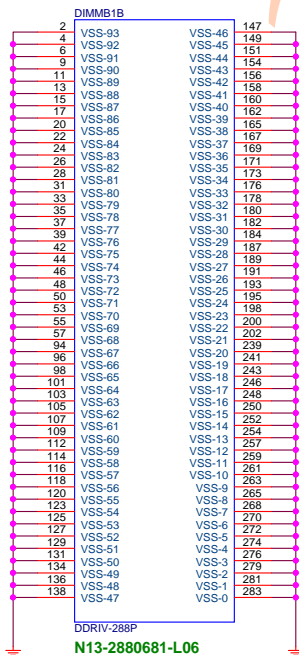
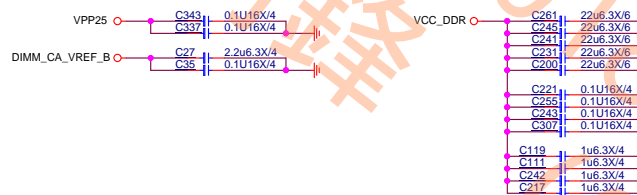
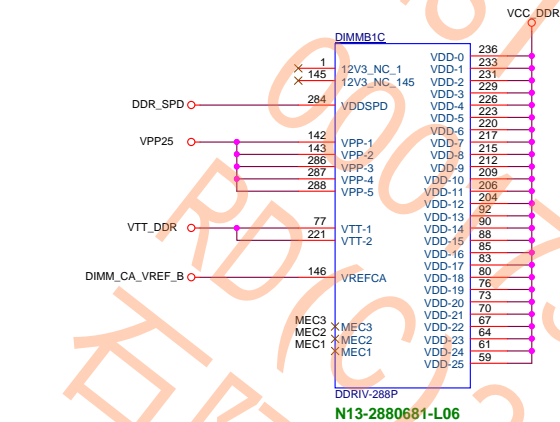




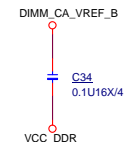
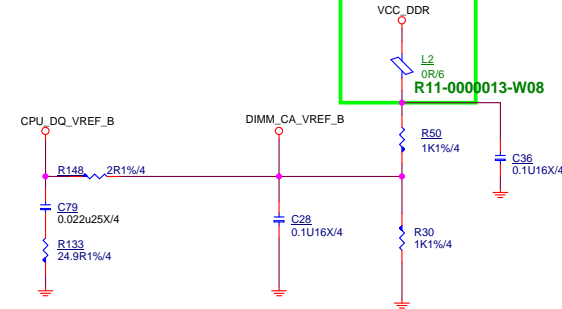








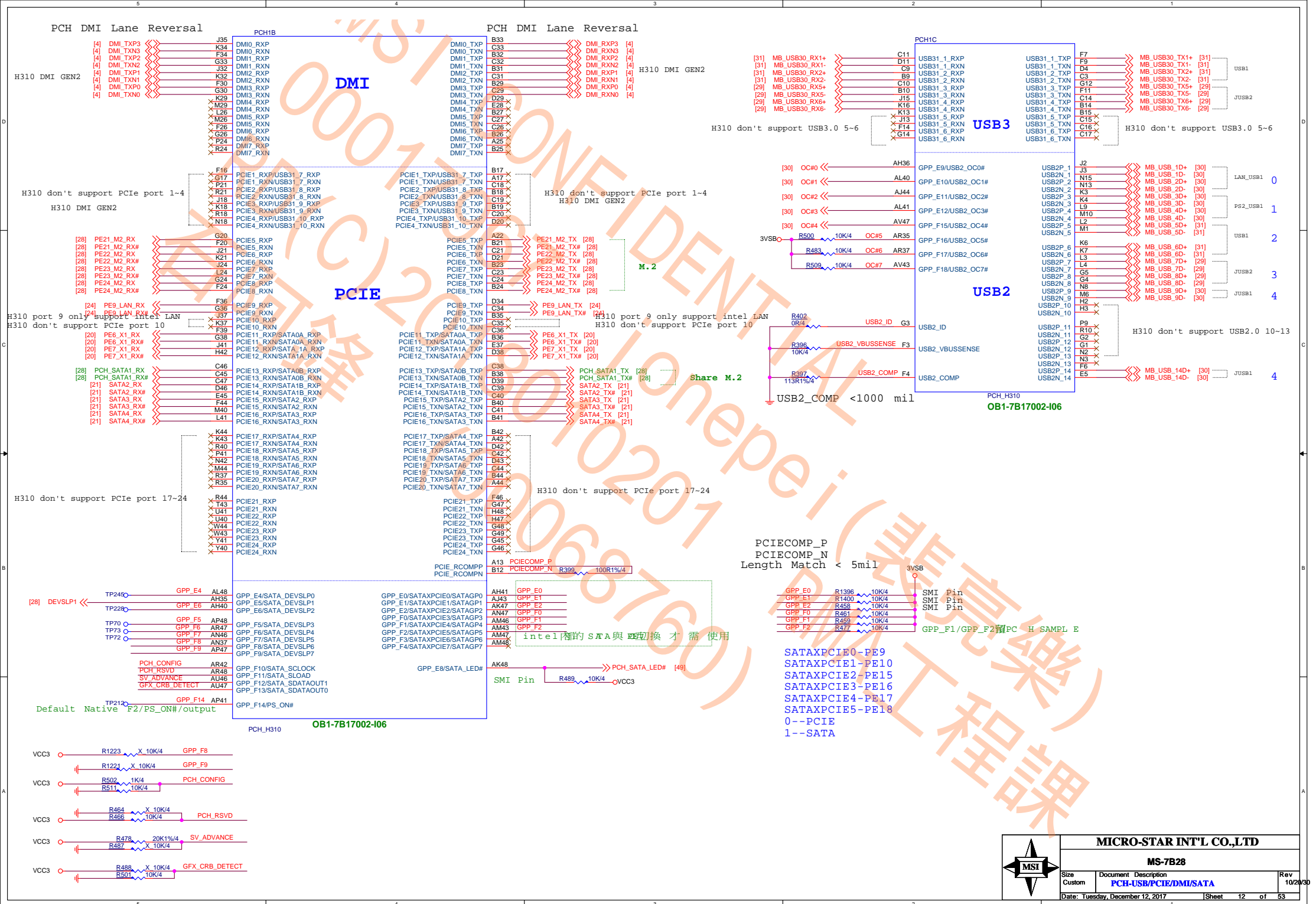
下一板直接短路



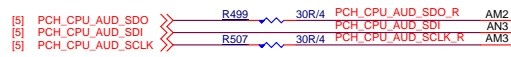
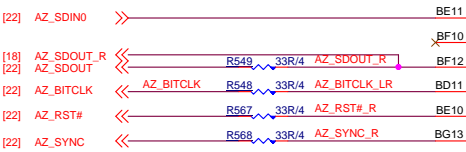
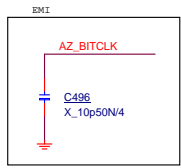
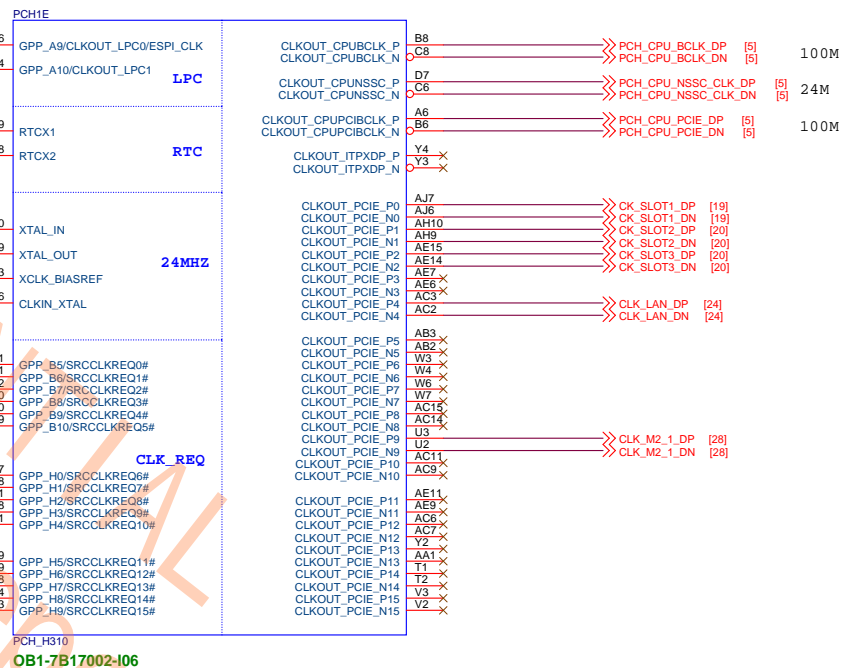
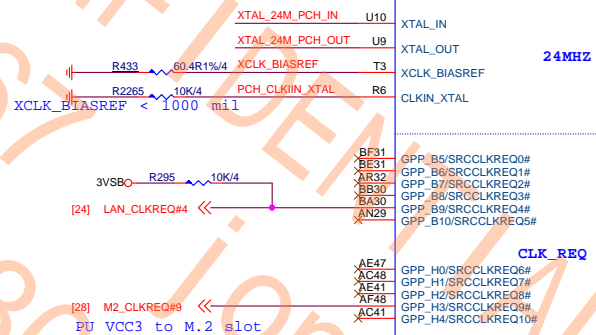
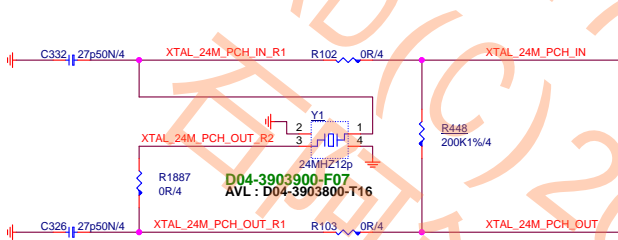
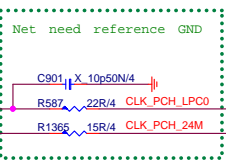
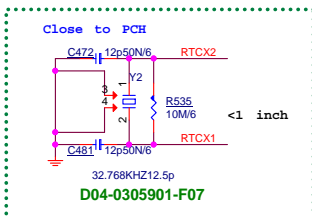
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Custom	DDR4-POWER/GND-2		10/20/30
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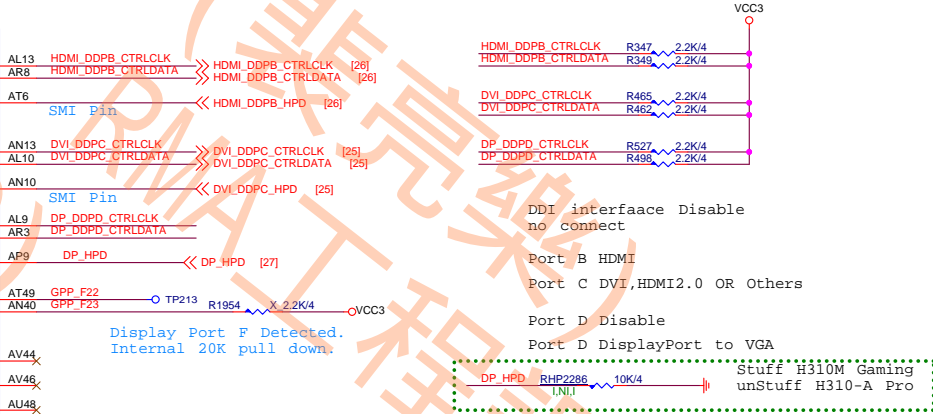
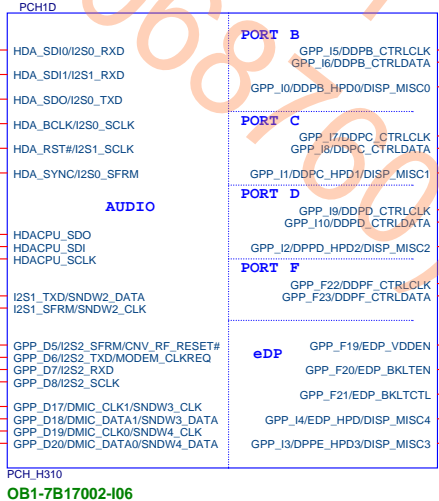


## RTC Block



Default Native F3/CNV\_RF\_R\_ESET#.

Default Native F3/MODEM\_CLKREQ.



Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V C

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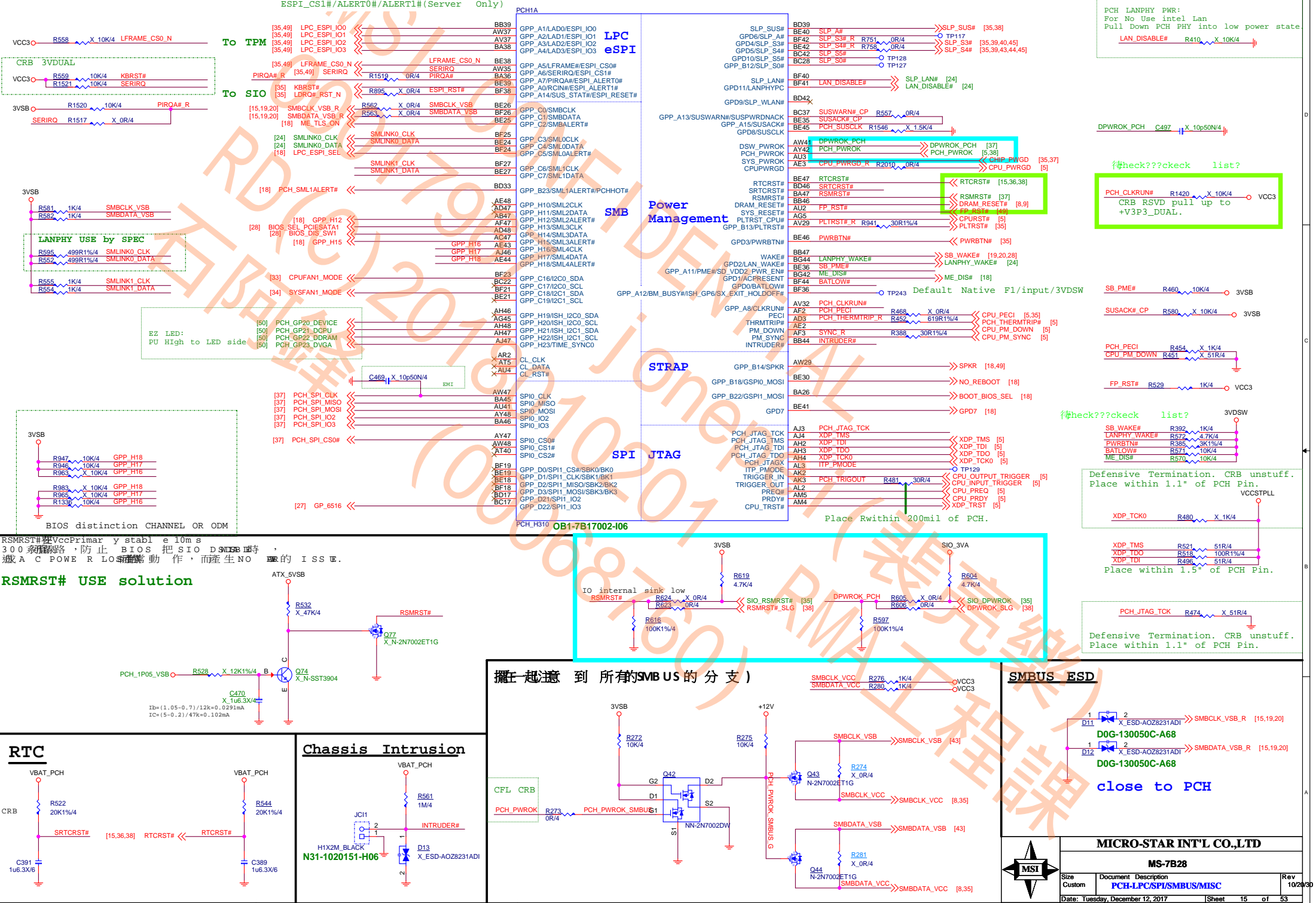
**MS-7B28**

Size	Document	Description	Rev
Custom		<b>PCH-Audio/Display/Clock</b>	10/20/30

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ESPI\_CS#/ALERT0#/ALERT1# (Server Only)

LANPHY USE by SPEC

RSMRST# USE solution

RTC

Chassis Intrusion

SMBUS ESD

MSI

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Size Custom Document Description Date: Tuesday, December 12, 2017 Sheet 15 of 53



VSS

OB1-7B17002-I06



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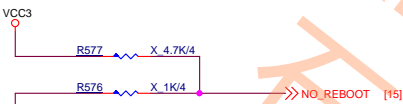
Size	Document	Description	Rev
Custom		PCH-GND	10/20/30
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TOP Swap



Internal pull-down 20K is disabled after PLTRST#

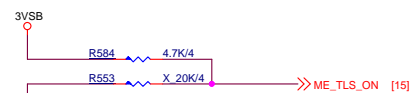
No Reboot



0 : DISABLE (Default)  
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

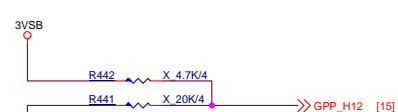
AMT and SBA with confidentiality



0 : DISABLE  
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

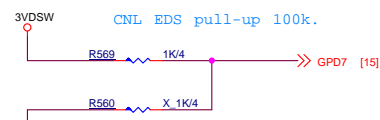
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING  
1 : SLAVE ATTACHED FLASH SHARING

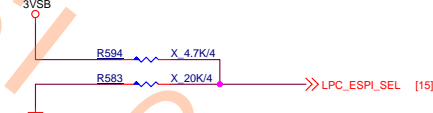
Internal pull-down 20K is disabled after RSMRST

Reserved



XTAL INPUT MODE  
0 = XTAL INPUT IS SINGLE-ENDED  
1 = XTAL INPUT IS DIFFERENTIAL  
PCH HAS INTERNAL 20K PD

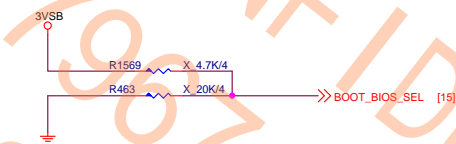
LPC eSPI Mode



0 : LPC  
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

Boot BIOS

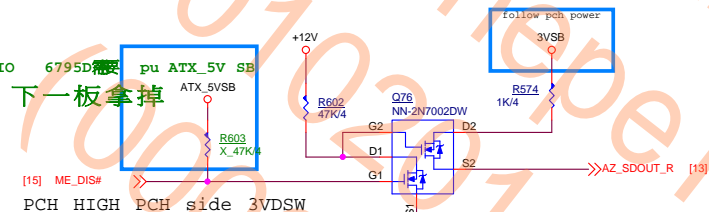


0 : SPI  
1 : LPC

Internal pull-down 20K is disabled after PLTRST#

HDA\_SDO

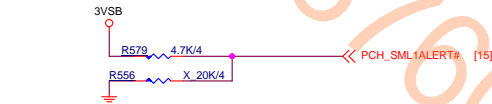
ME flash by GPIO



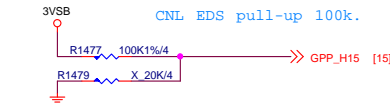
[15] ME\_DIS#

PCH HIGH PCH side 3VDSW

Reserved

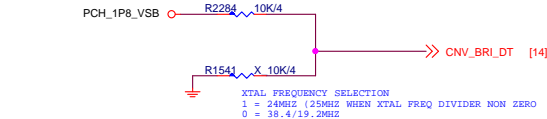


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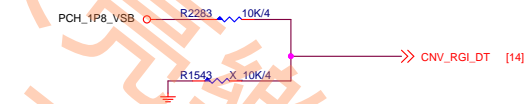


VCCSPI 3.3V, Internal pull-down.

SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE  
0 = VCCSPI IS CONNECTED TO 3.3V RAIL - DEFAULT  
1 = VCCSPI IS CONNECTED TO 1.8V RAIL  
PCH HAS INTERNAL 20K PD



XTAL FREQUENCY SELECTION  
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO)  
0 = 38.4/19.2MHZ



CNL EDS  
1 = Integrated CNVi enable  
0 = Integrated CNVi disable

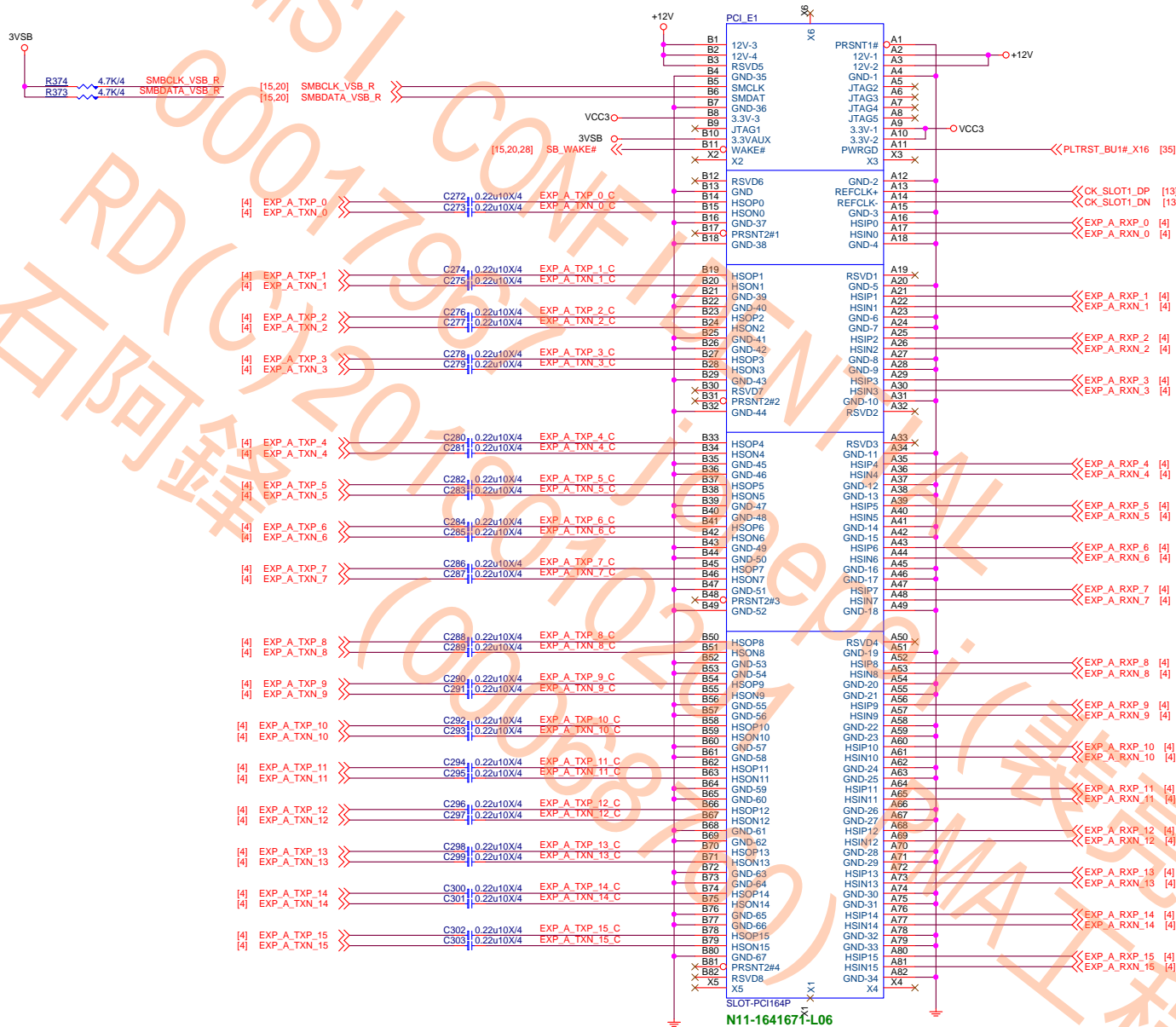
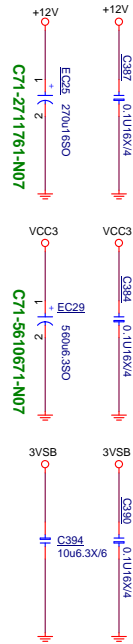


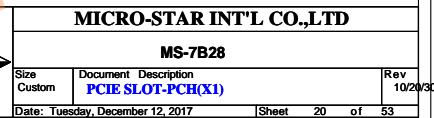
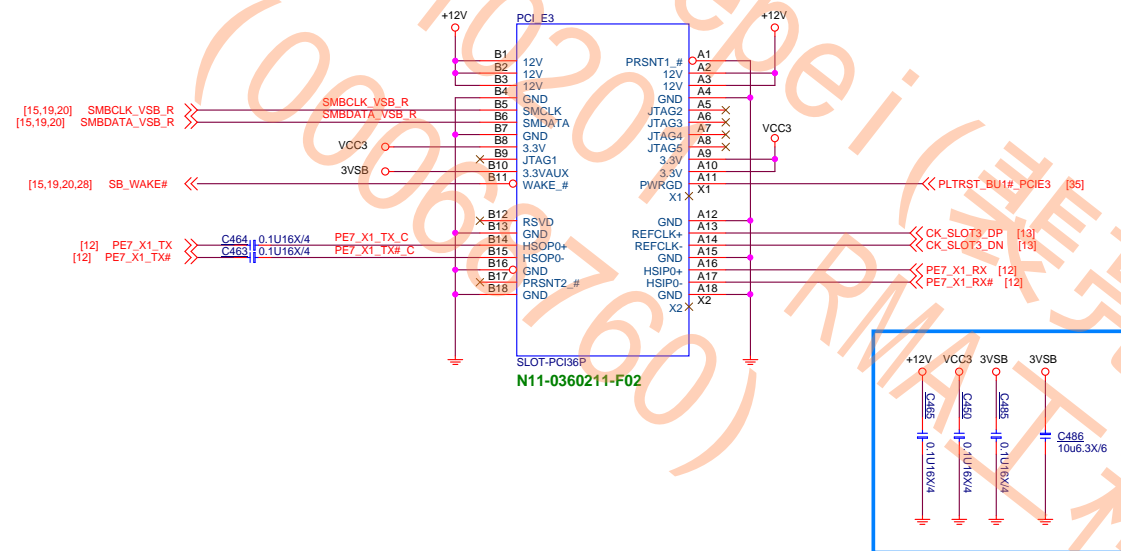
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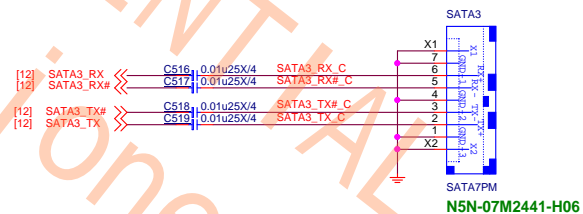
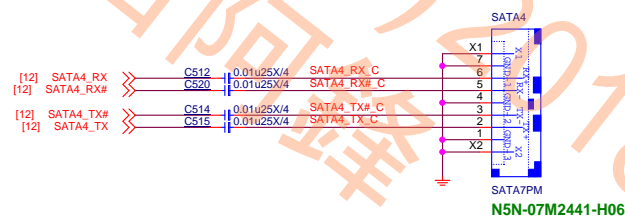
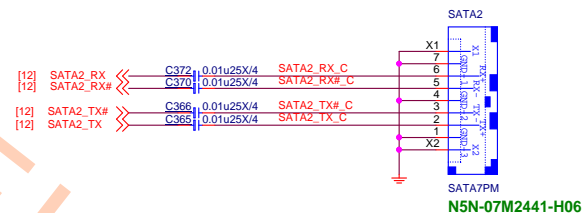
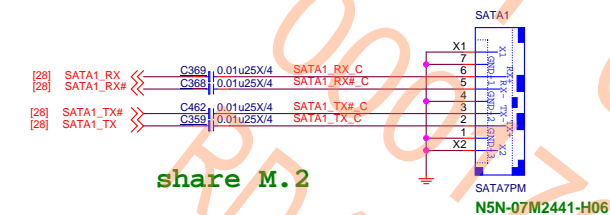
Size	Document	Description	Rev
Custom		PCH-Strap	10/20/30
Date:	Tuesday, December 12, 2017	Sheet	18 of 53







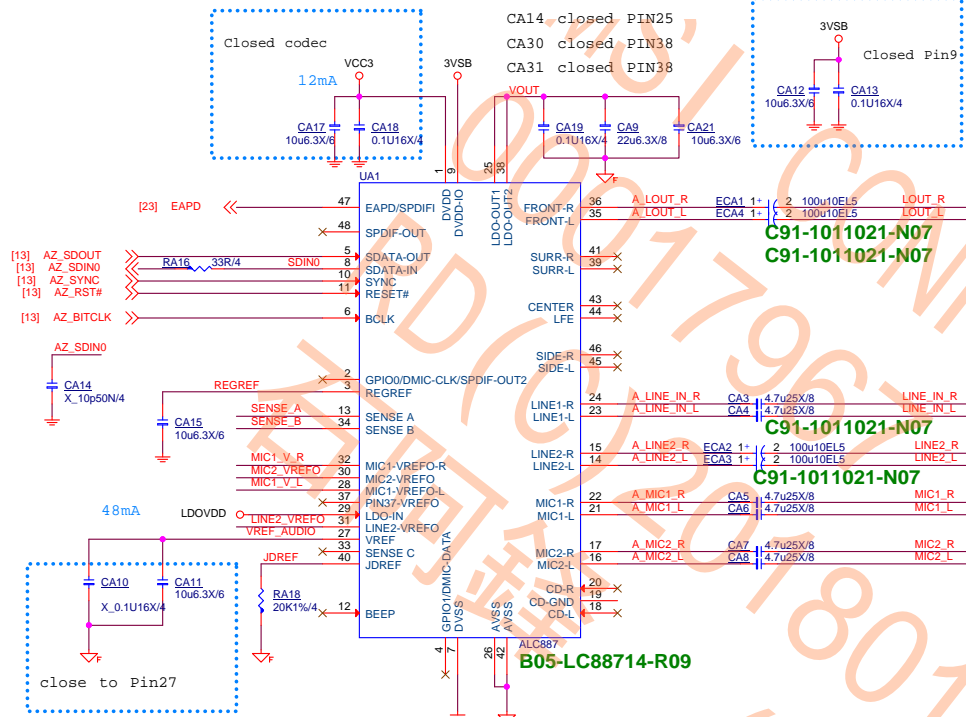
# SATA 6G



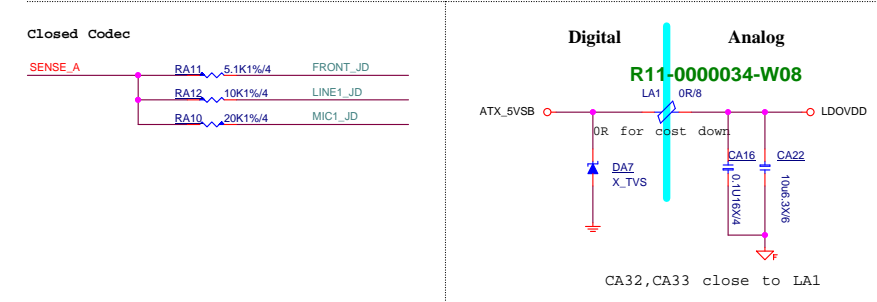
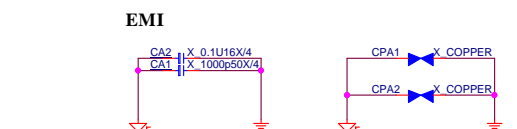
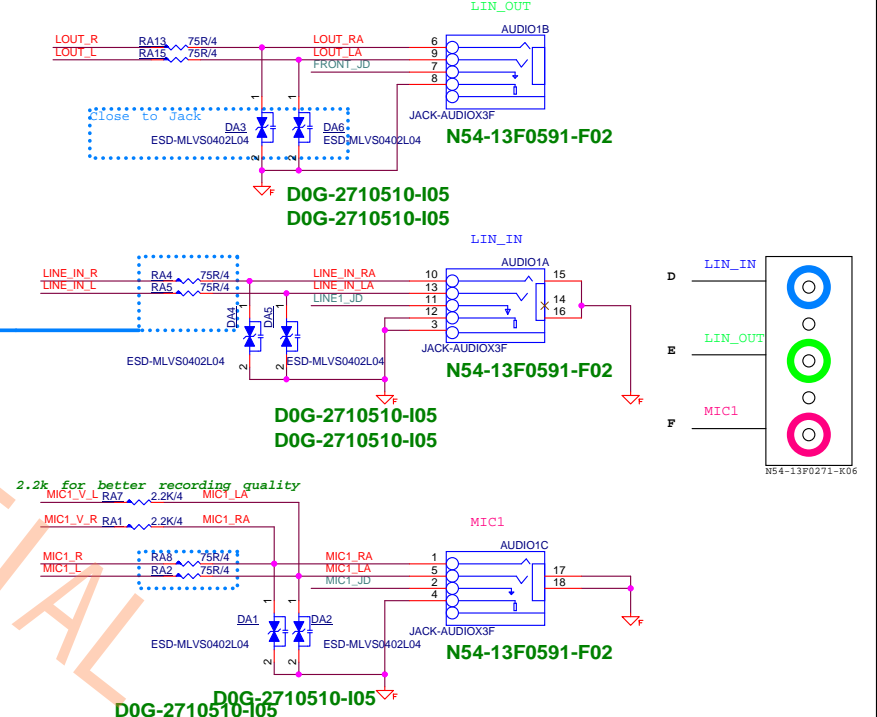
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MS-7B28

Size	Document	Description	Rev
Custom		SATA connector	10/2/30
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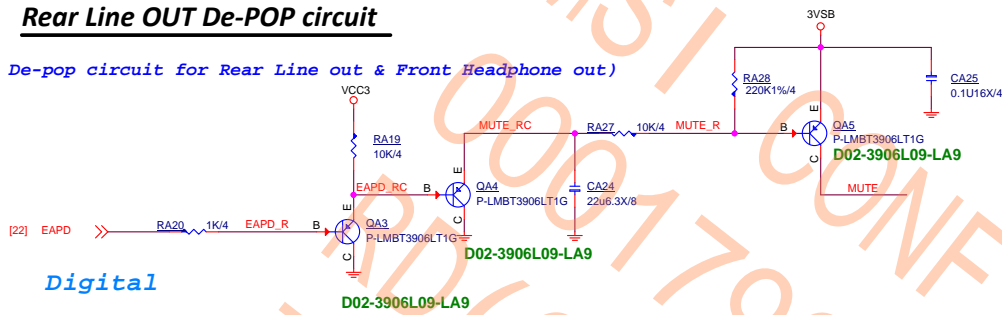


for rear I/O 6port:  
887VD/892:1k  
for rear I/O 3port:  
887VD/892:75R



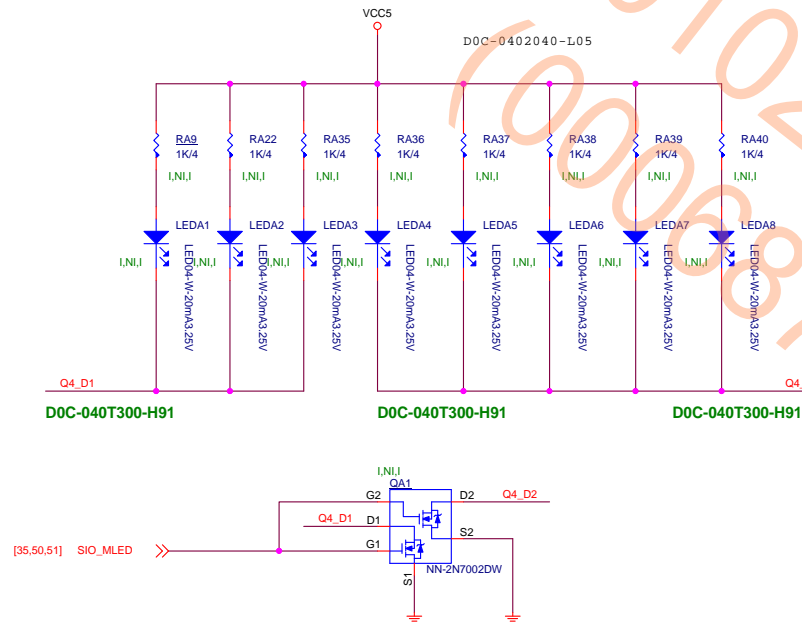
## Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Audio moat is transparent and width 40mil

## Audio LED



Schematic Cfg	Project	
CFG1-7B38-H310 (H310M GAMING PLUS)	ver.1.0	V A
CFG1-7B38-H310-APRO (H310-A Pro)	ver.2.0	X B
CFG1-7B38-H310 (H310-A GAMING ARCTIC)	ver.3.0	V C



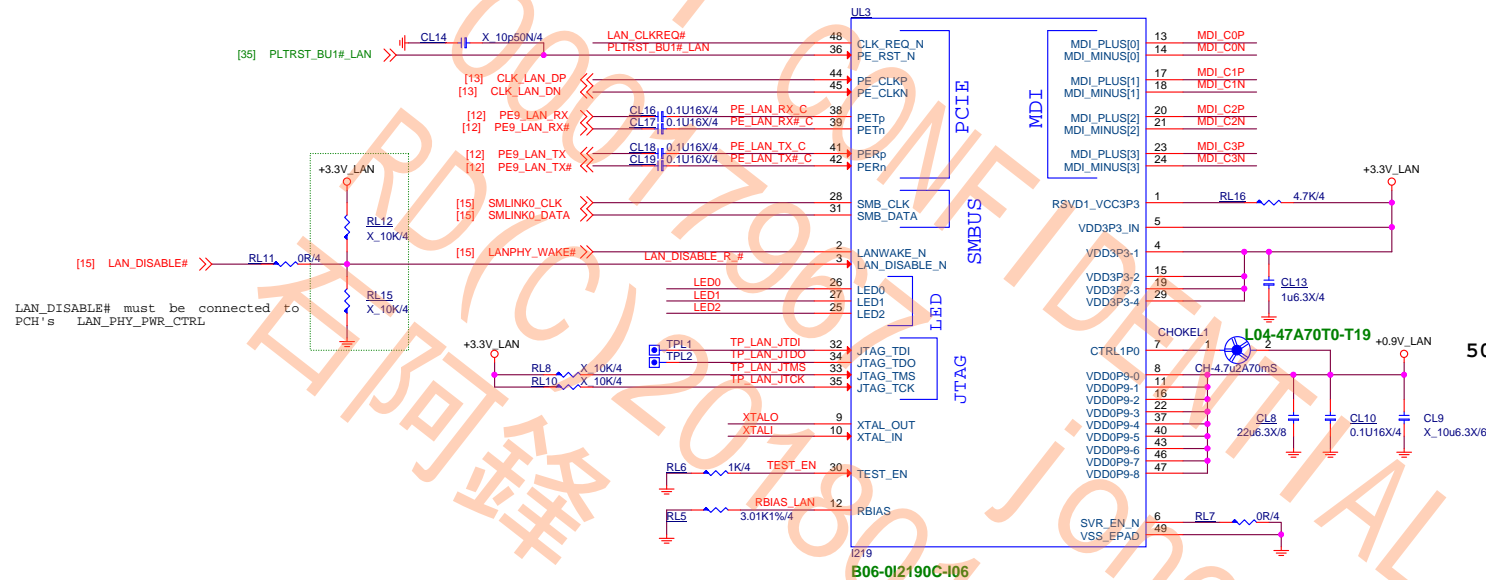
MICRO-STAR INT'L CO.,LTD

MS-7B28

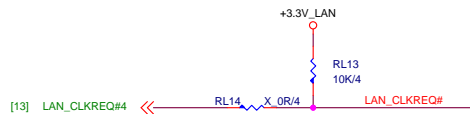
Size	Document	Description	Rev
Custom		AUDIO - depop circuit	10/20/30
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## Intel Lan- I219

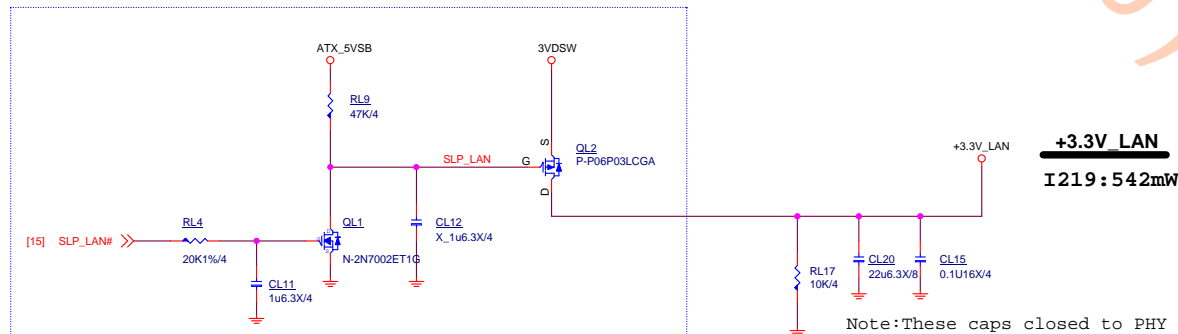


PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port.  
If CLK\_REQ\_N is not used, pin48 is pulled up 10KR to 3.3V\_LAN

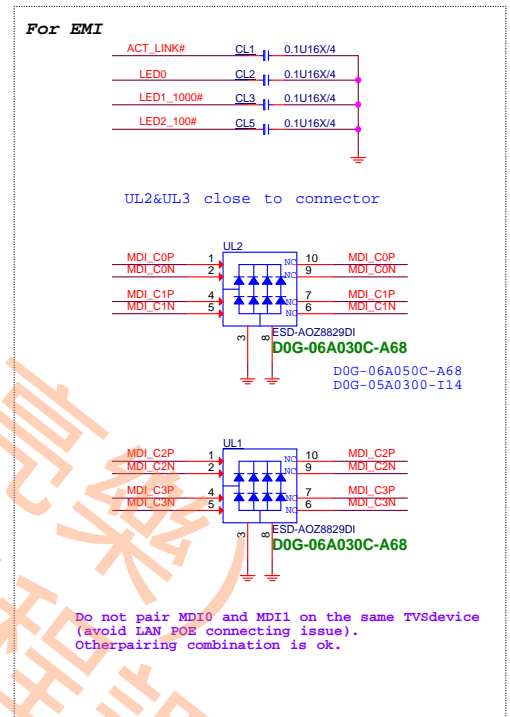
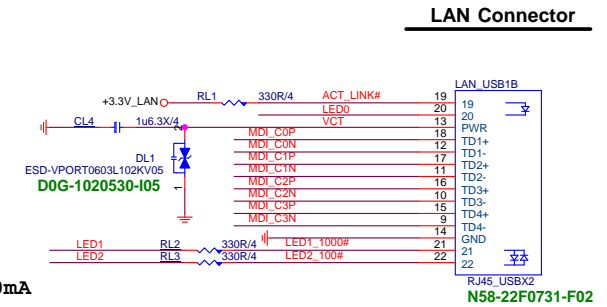


The 10Kohm pull-up resistor (RL18) of CLK\_REQ\_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:  
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



Note: These caps closed to PHY

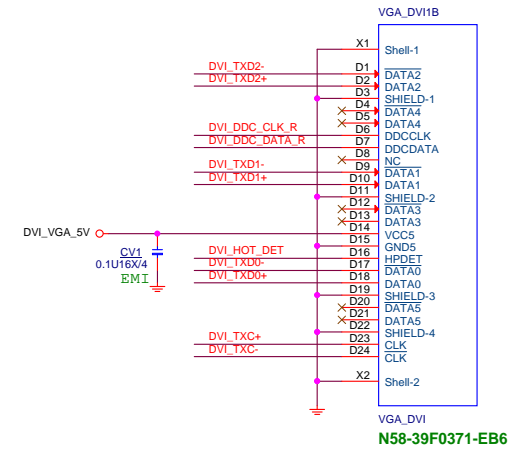


**MICRO-STAR INT'L CO.,LTD**

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VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



[13] DVI\_DDPD\_HPD

VCC3

R225 10K/4

C123 X\_0.01u25X/4

VCC5

R224 10K/4

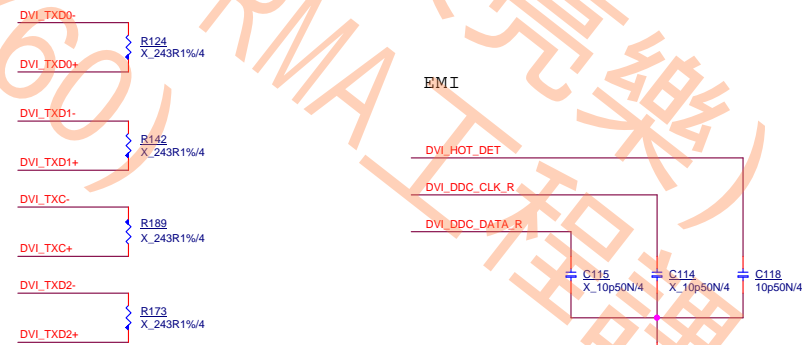
Q24 NPN-LM8T3904DW1T1G

R222 10K/4

R220 100K/4

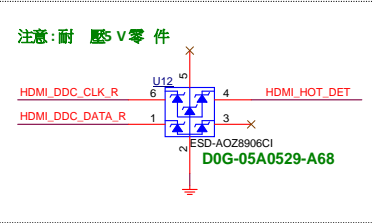
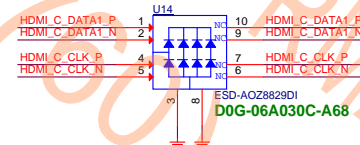
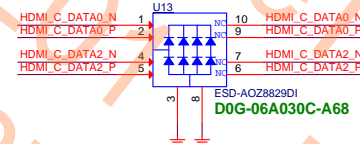
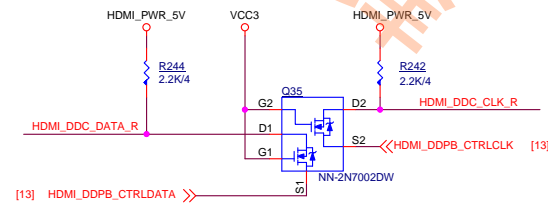
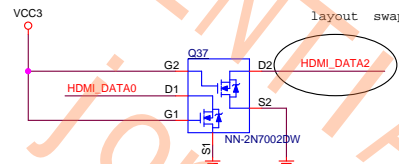
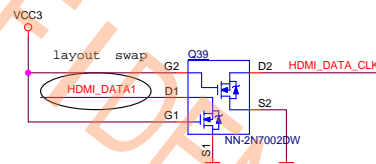
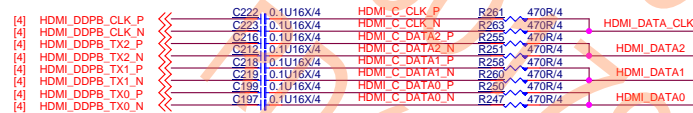
C117 0.01u25X/4

DVI\_HOT\_DET

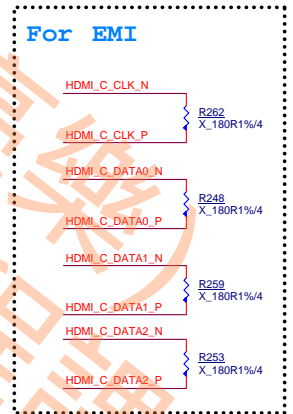
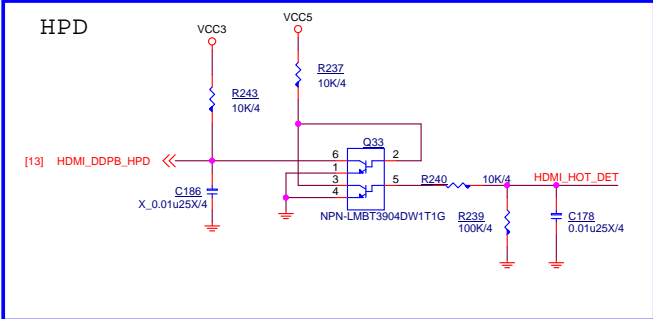
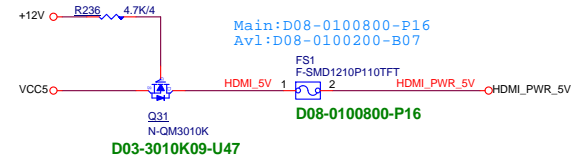
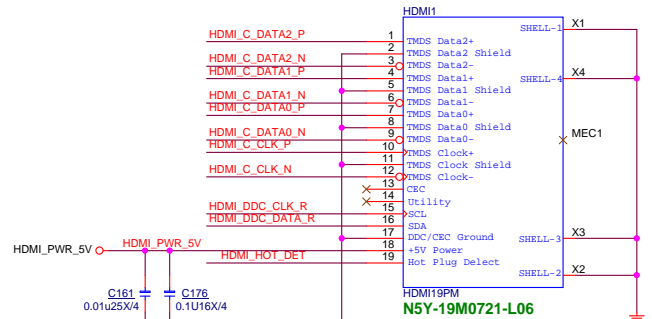


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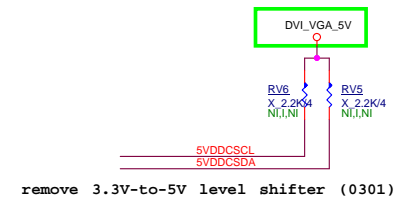
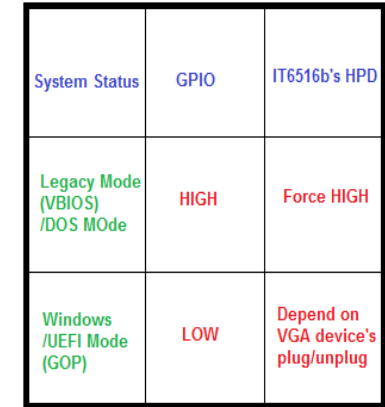
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



注意:耐 壓5V零件



If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

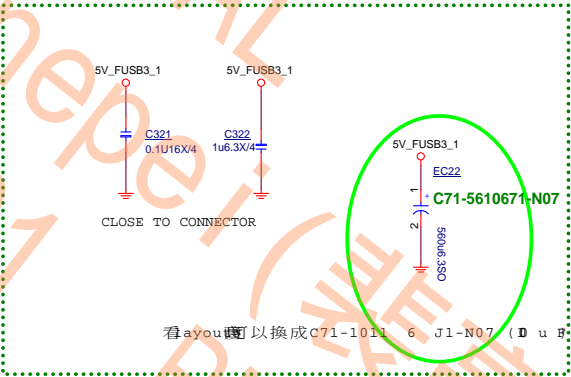
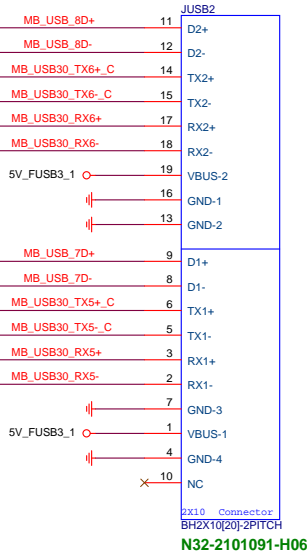
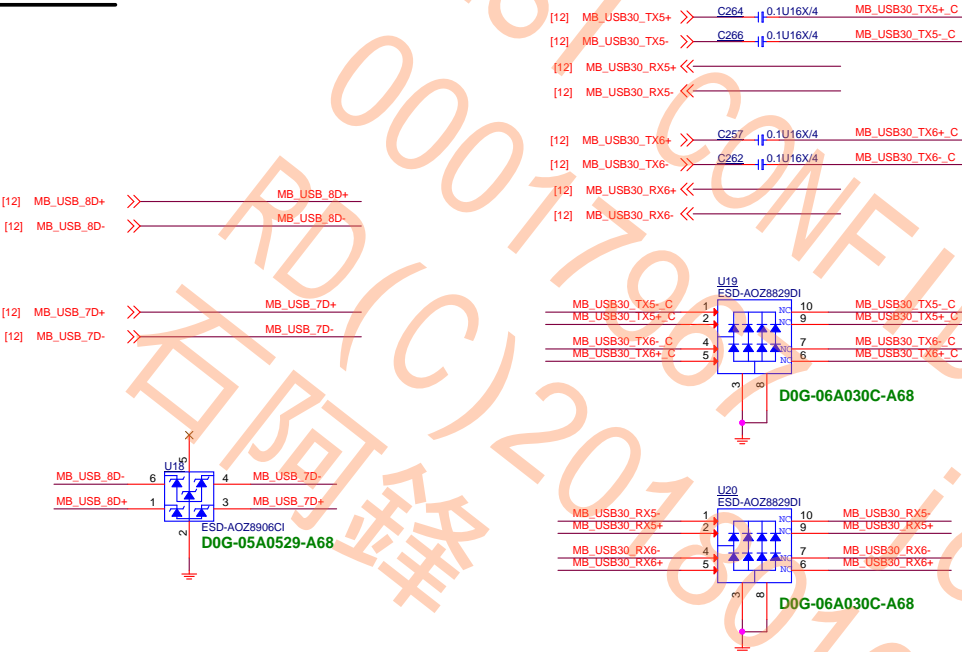


Size Custom	Document Description <b>VGA - IT6516</b>	Rev 10/20/30
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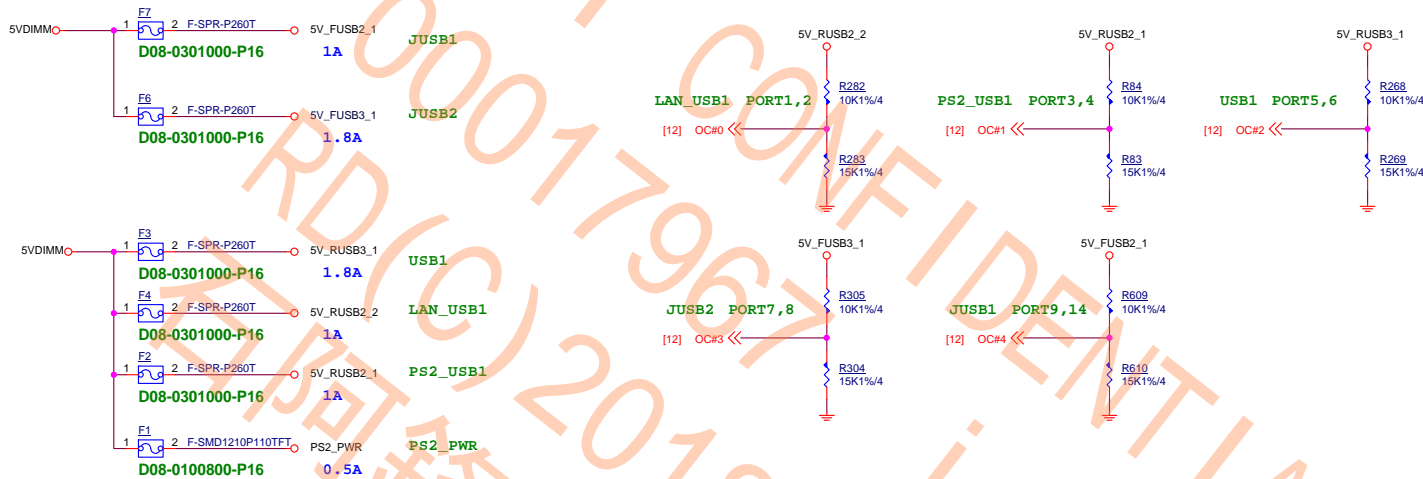
Front JUSB3 port 7,8



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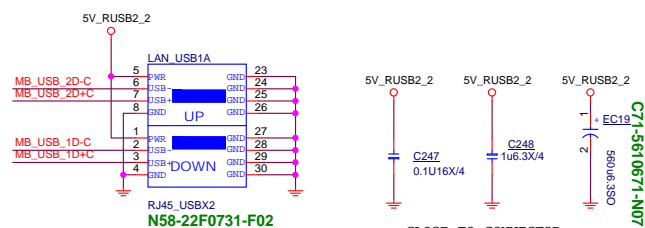
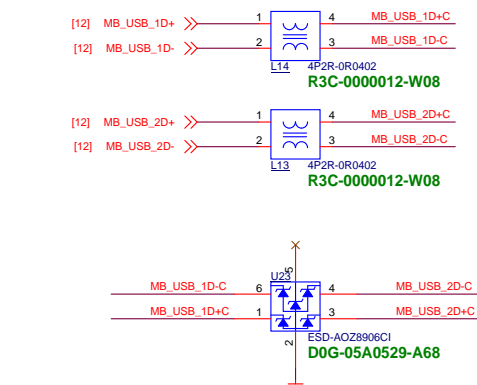
MS-7B28

Size	Document	Description	Rev
Custom		Front USB3.0 Connector	10/20/30
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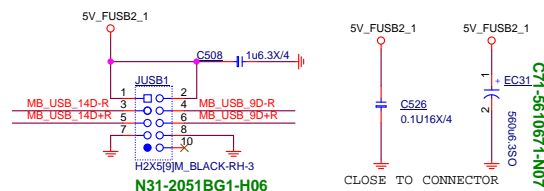
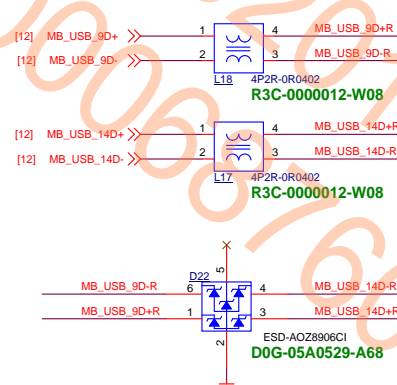


USB CONN	USB POWER	PCH PORT	OC# SIGNAL
LAN_USB1	5V_RUSB2_2	Port1,2	OC#0
PS2_USB1	5V_RUSB2_1	Port3,4	OC#1
USB1	5V_RUSB3_1	Port5,6	OC#2
JUSB2	5V_FUSB3_1	Port7,8	OC#3
JUSB1	5V_FUSB2_1	Port9,14	OC#4

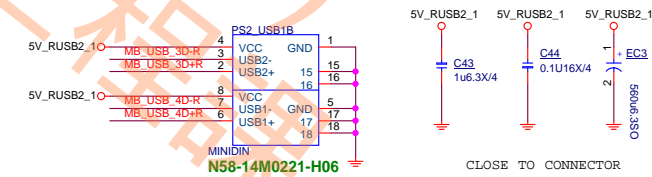
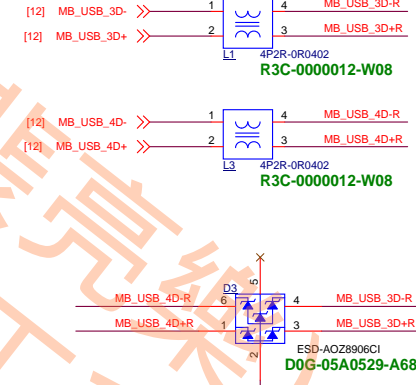
#### Rear USB1 port 1,2



#### JUSB1 PORT 9,14

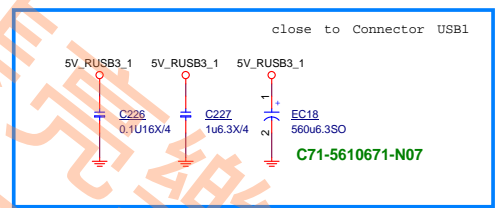
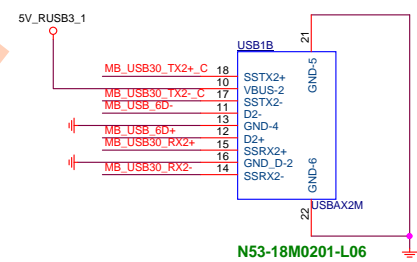
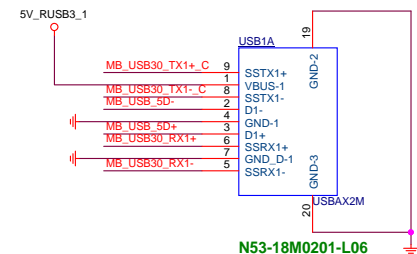
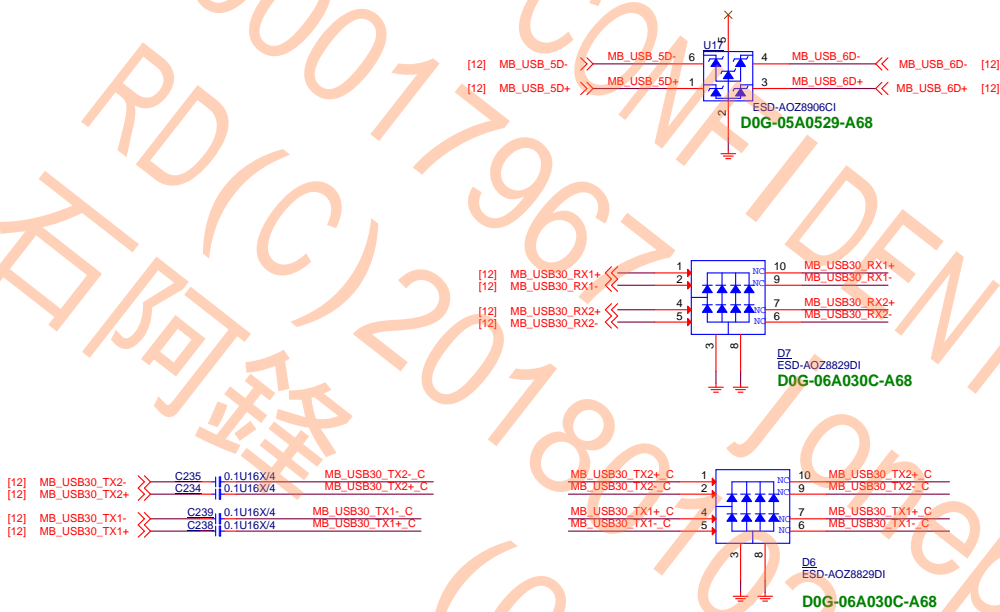


#### PS2\_USB1 PORT 3,4

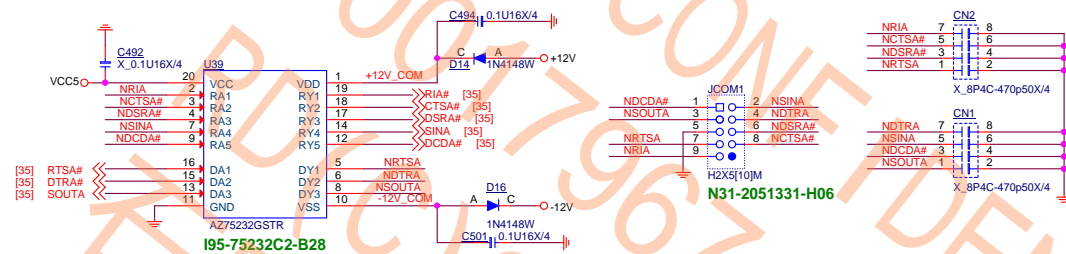


MICRO-STAR INT'L CO.,LTD			
MS-7B28			
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Custom		USB2.0 Connector	10/20/30
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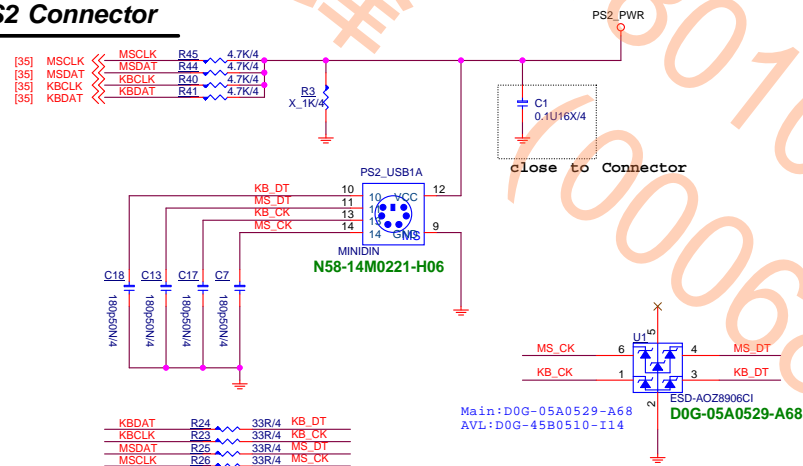
# REAR USB1 Connect



## SERIAL PORT 1



## PS2 Connector



MICRO-STAR INT'L CO.,LTD

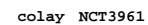
MS-7B28

Size	Document	Description	Rev
Custom	SERIAL POR/PS2		10/29/30
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GPIO 自由切換 PW M/DC MO DE



Internall pull up 1.65V



```
default
OC SET By PM SPEC
20170428
```



Avoid NCT3947S MODE PIN Leakage

VCC3

R81  
X\_10K/4

SYSFAN1 FIX\_MODE

R82  
X\_10K/4

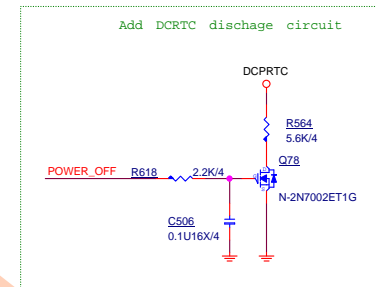
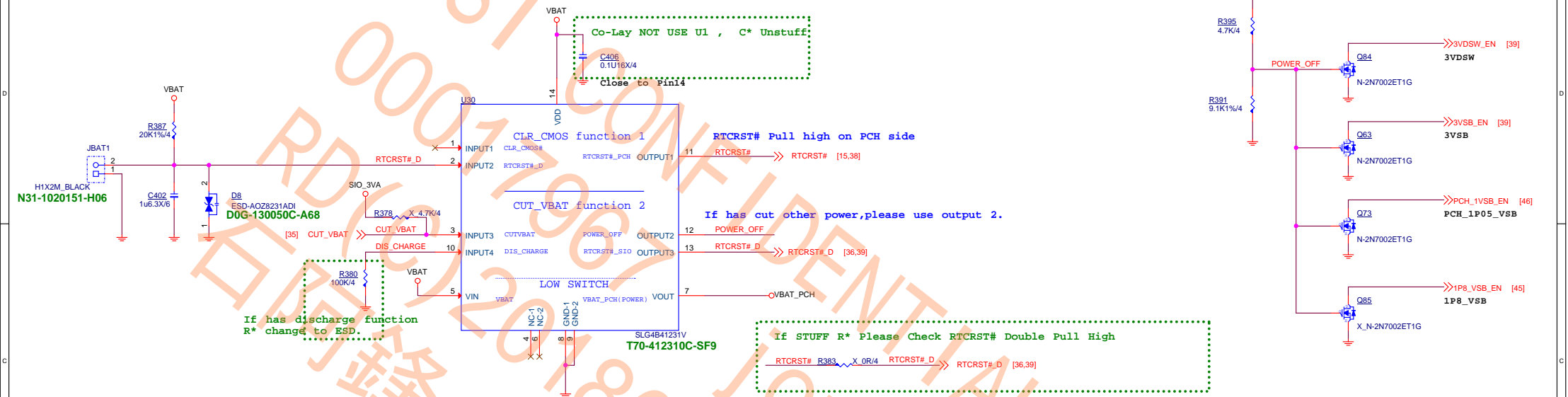
C55  
1u6.3X/4



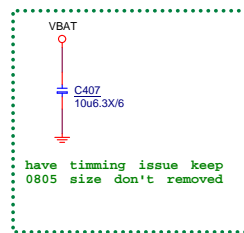
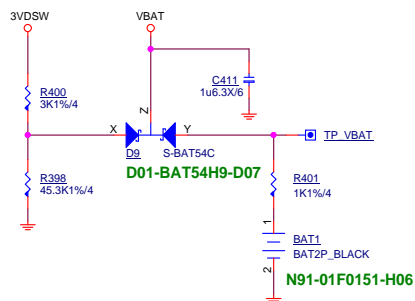




## Cut VBAT



## VBAT



Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

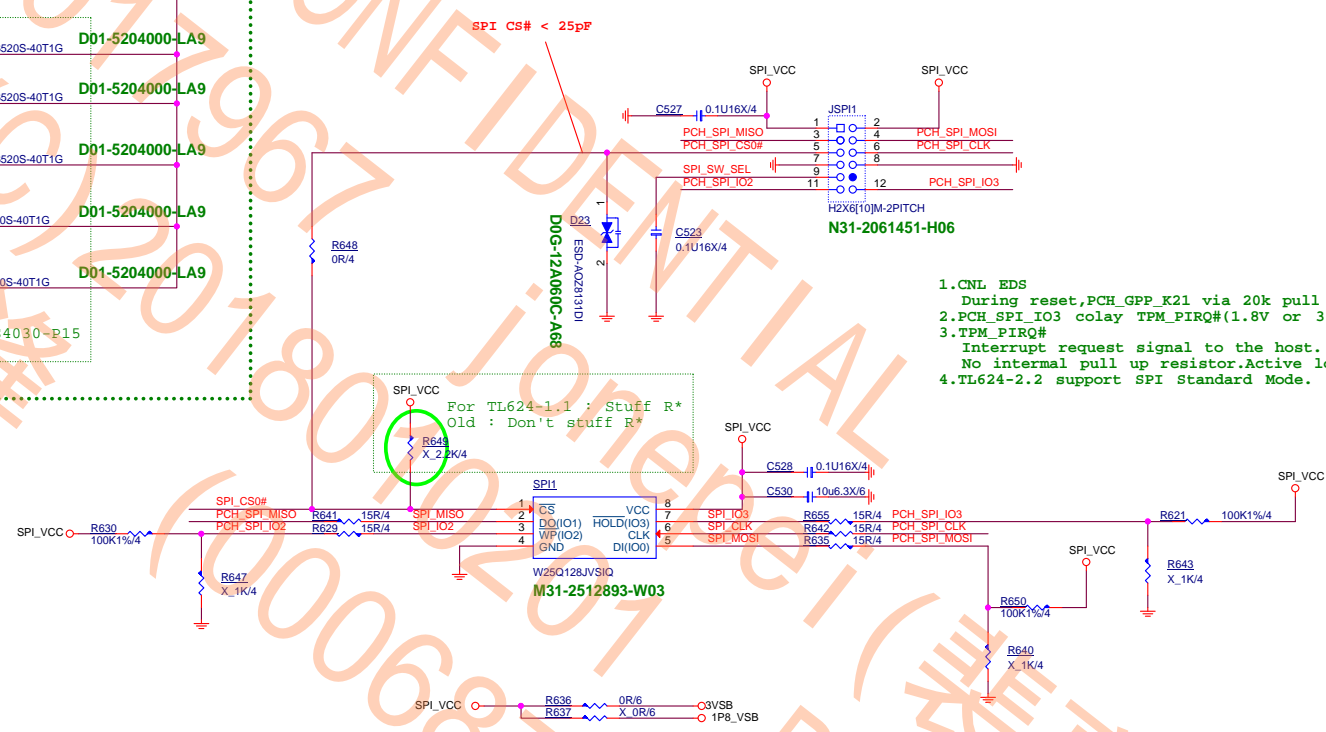
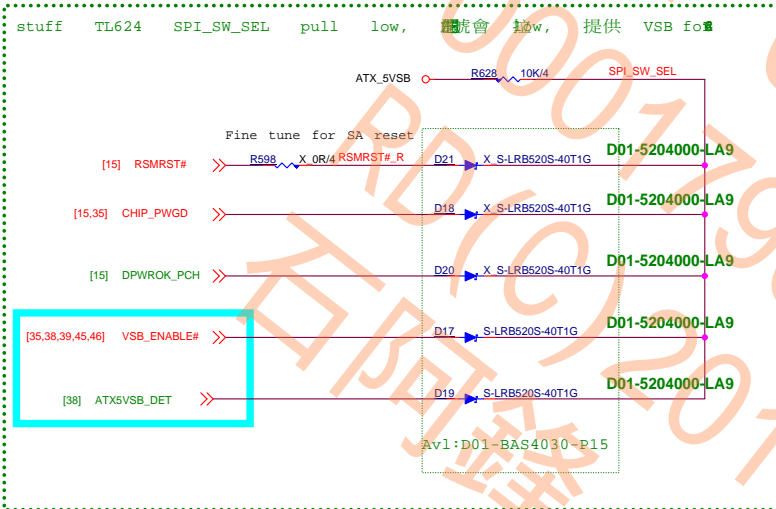
Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default



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Custom		CUT VBAT circuit	10/2/30
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[15] PCH\_SPI\_MOSI << PCH\_SPI\_MOSI  
[15] PCH\_SPI\_MISO << PCH\_SPI\_MISO  
[15] PCH\_SPI\_CLK << PCH\_SPI\_CLK  
[15] PCH\_SPI\_CS0# << PCH\_SPI\_CS0#  
[15] PCH\_SPI\_IO2 << PCH\_SPI\_IO2  
[15] PCH\_SPI\_IO3 << PCH\_SPI\_IO3

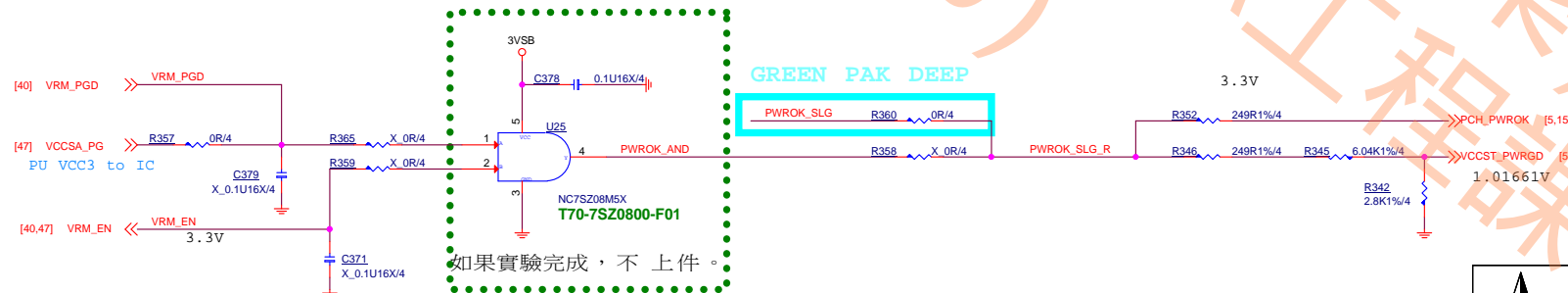
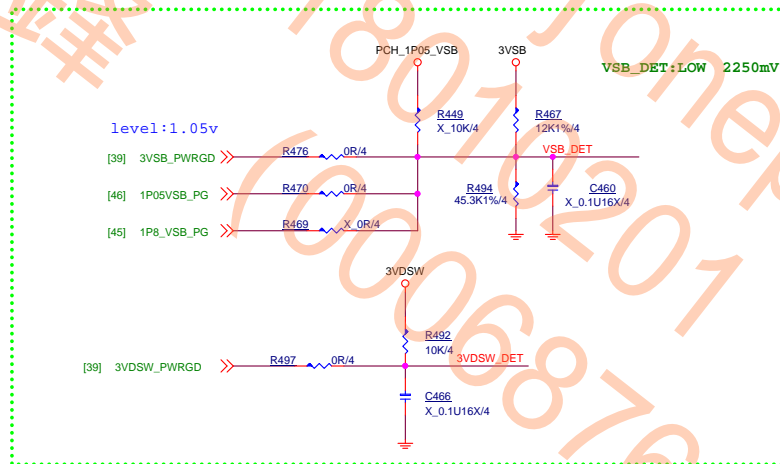
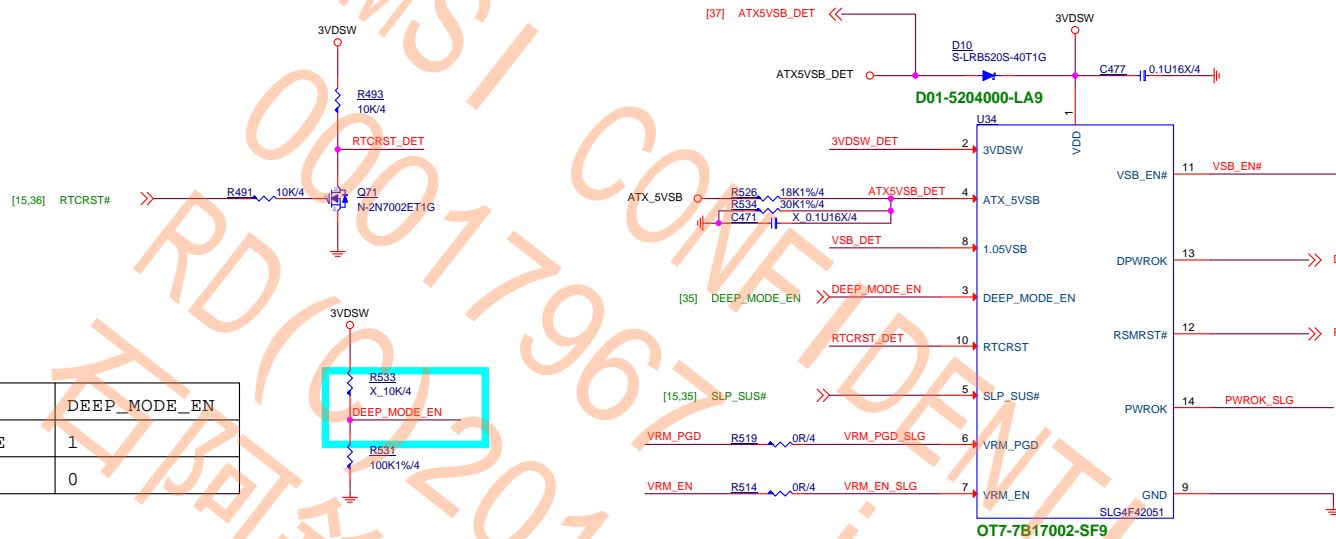


- 1.CNL EDS  
During reset,PCH\_GPP\_K21 via 20k pull up to 3.3V.
- 2.PCH\_SPI\_IO3 colay TPM\_PIRQ#(1.8V or 3.3V,OD)
- 3.TPM\_PIRQ#  
Interrupt request signal to the host.  
No internal pull up resistor.Active low.
- 4.TL624-2.2 support SPI Standard Mode.



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Custom		BIOS ROM	10/29/30
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	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0



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Custom		GREEN PAK DEEP	10/2/30
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[illegible]

AVL: I31-0866509-A36  
I31-7116S09-N03

ATX\_5VSB

C416 1u6.3X/4

U31 GS7116S5

VDD VOUT

EN GND ADU

1 2 3 4 5

SIO\_3V\_A

C421 X 0.1uF6X/4

3V\_A\_FB

VFB=0.8

R1 R403 10K1%/4

R2 R407 3.16K1%/4

C422 10u6.3X/6

[36] RTCRSts\_D

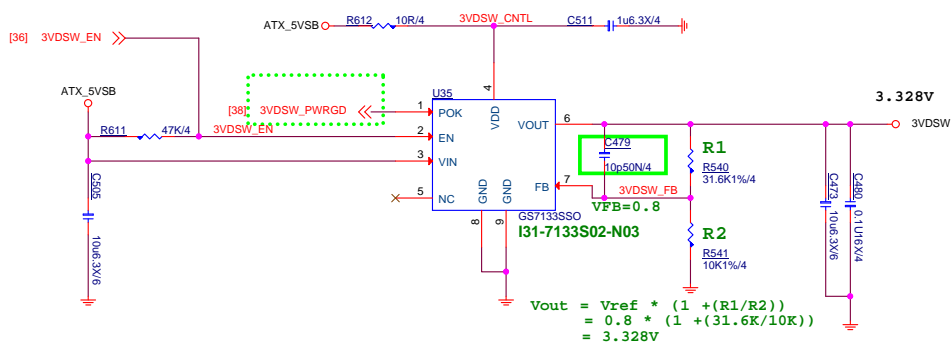
R393 OR/4

SIO\_3V\_A\_EN

C413 X 1u6.3X/4

Vout = Vref \* (1 + (R1/R2))  
= 0.8 \* (1 + (10K/3.16K))  
= 3.33V

Intel Lan 不用小顆 C，因為瞬間電流會很大。  
113mA(PCH)+0.6mA(RTC)+200mA(LAN-I219)+SIO



VDDUAL is power source of 1P0SB, 1.8PSB & 3VSB

VCC5 5VSB 5V 3VSB

[35,39,49] ATX\_PWR\_OK

[15,35,39,40,45] SLP\_S3#

[15,35,39,43,44,45] SLP\_S4#

ATX\_5VSB

[35,37,38,39,45,46] VSB\_ENABLE#

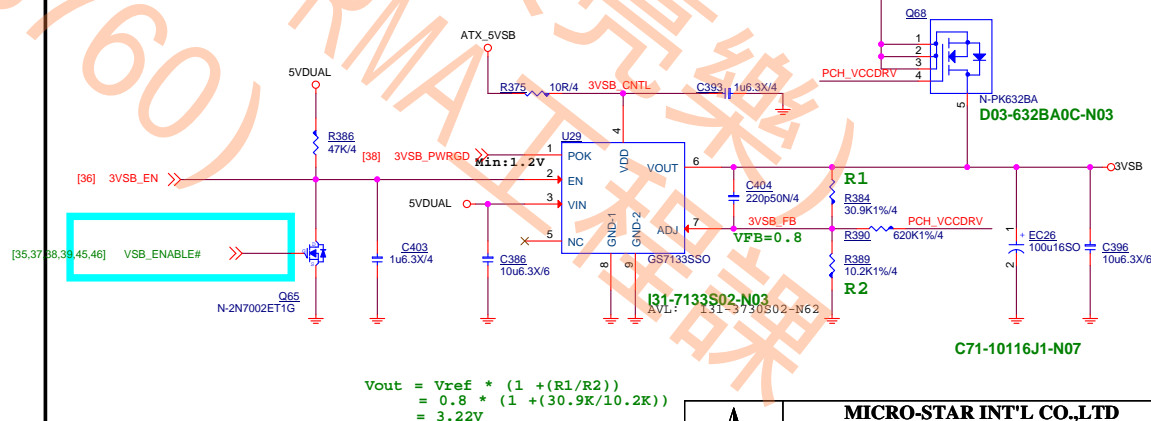
7501 Mode

H:Support S0/S3/S5

L:Support S0/S3

ATX\_5VSB

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC5 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC5 not ready and let the 3VSB sequence fail.

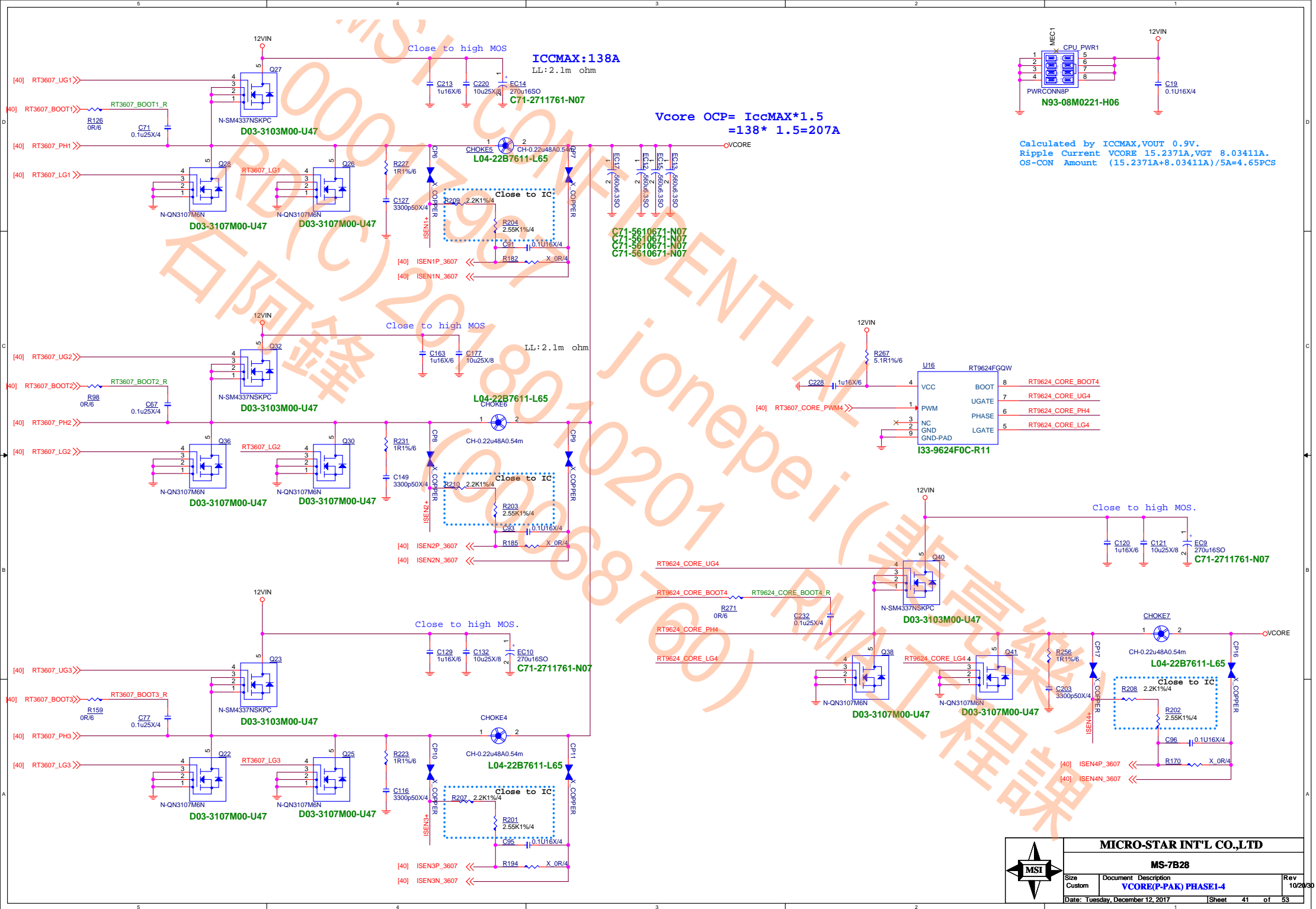
$$2.156A(\text{PCH}) + 1.125A(\text{PE SLOT} * 3)$$


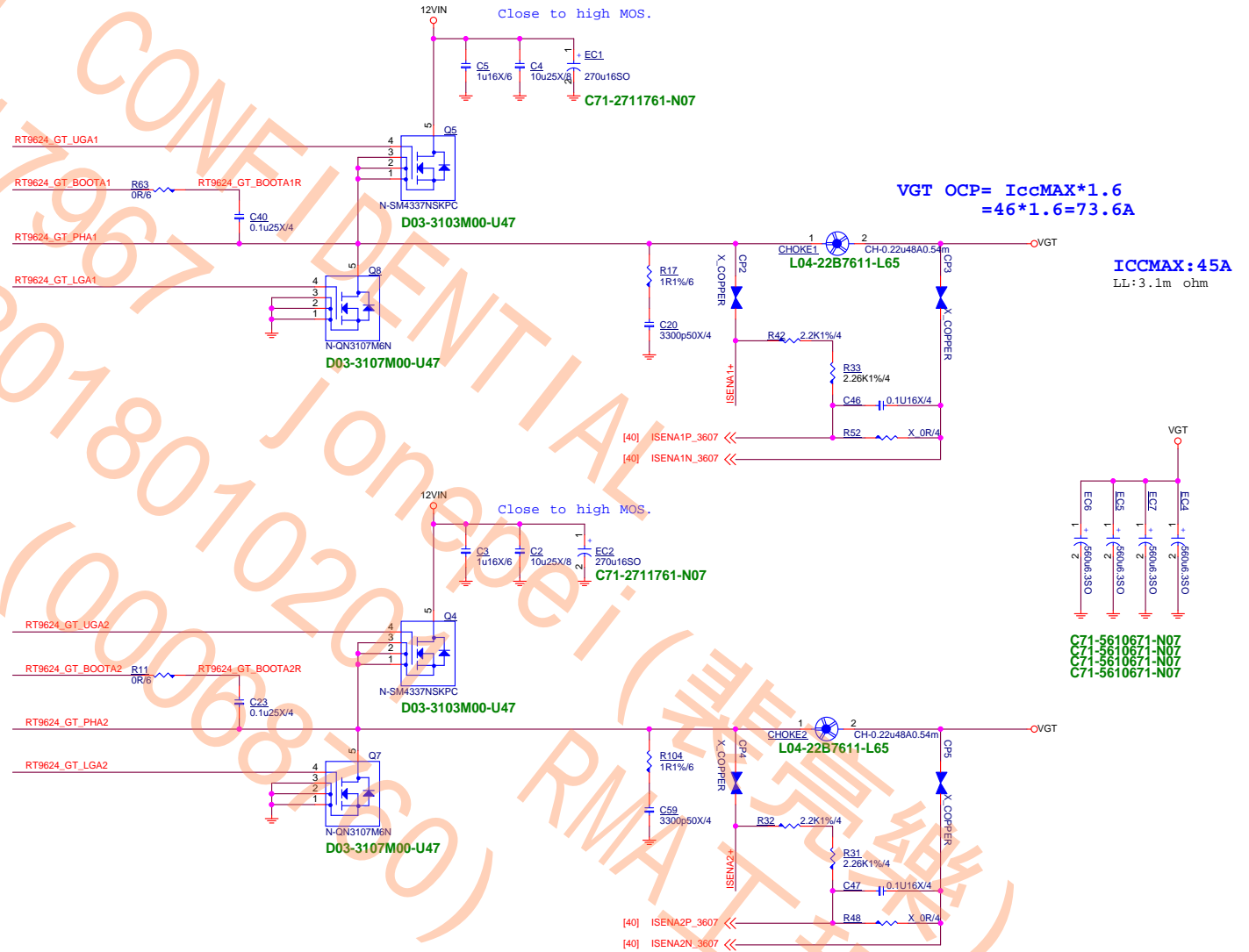
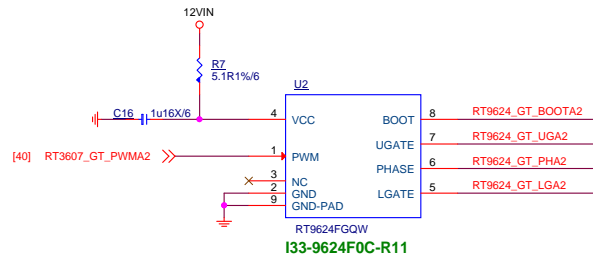
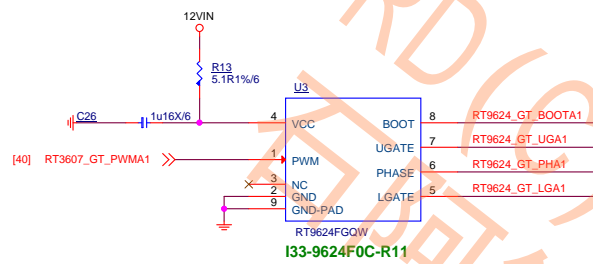
MS-7B28

Size Custom	Document Description <b>ACPI CONTROLLER</b>	Rev 10/20/30
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# VCC\_DDR@1.2V/11.525A

$$DDR4\_1.2V\ 3.3A+7.85A+0.375A=11.525A$$

3.3A FOR CPU  
10A FOR 2DIMM DDR4  
0.375A FOR VTT\_DDR

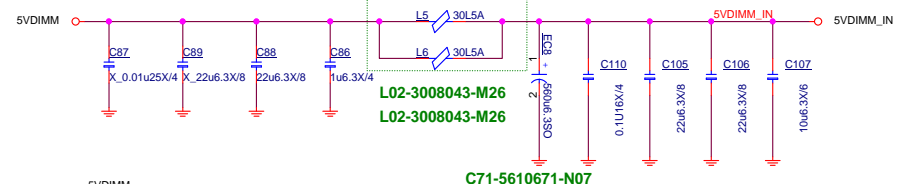
$$R_{limit} = I_{limit} * R_{ds} * 10 / 5uA$$

$$R_{limit} = 14.9825 * 4 * 10 / 5$$

D03-632BA0C-N03  
Current limit=  $118K * 5uA / (10 / 4mohm) = 14.75A$   
 $0.4V < R_{limit} * 5uA < 3V$

VID	Reference Voltage (V)
H	0.675
L	0.75

Input Current=  $(11.525A * 1.2V) / 5V / 0.8 = 3.4575A$   
L02-3008043-M26  
Over 85°C Rated Current 1.5A.



$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 11.525 * 0.427$$

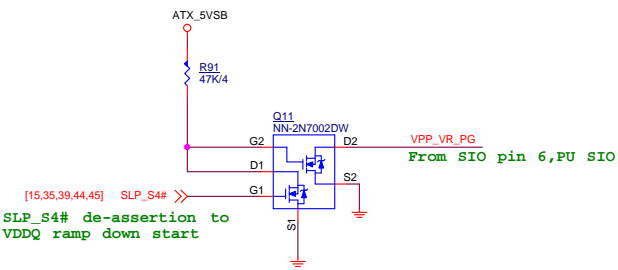
$$= 4.921175A$$

$$DDR\ OCP = R_{44} * 5uA / 10 / D_{ds}(on)$$

$$138k * 5uA / 10 / 3m = 23A$$

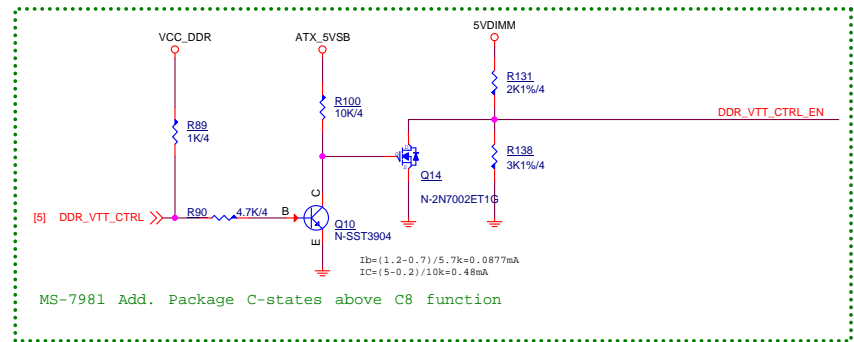
$$138k * 5uA / 10 / 4.6m = 15A$$

MOS  $R_{ds}(on)$  是  $m \sim 4.6m\ ohm$



[15,35,39,44,45] SLP\_S4#  
SLP\_S4# de-assertion to VDDQ ramp down start

VPP ramp down after VDDQ ramp down

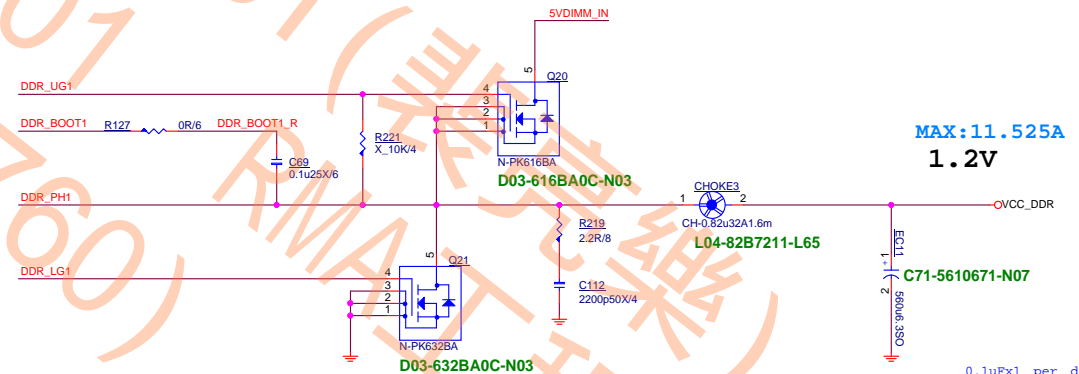


MS-7981 Add. Package C-states above C8 function

$$V_{out} = V_{ref} * (1 + (R1/R2))$$

$$= 0.75 * (1 + (1K/1.65K))$$

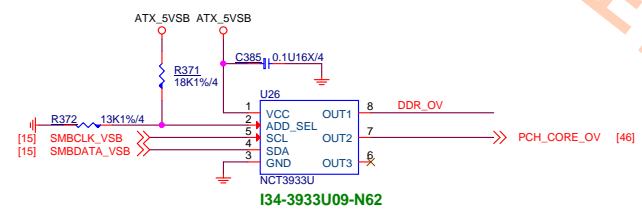
$$= 1.204V$$



MAX:11.525A  
1.2V

## UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



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Custom		DDR-RT8231	10/29/30
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# VPP25 @2.5V/2A

2DIMM :1.12A FOR  
DDR VPP2.5V

DDR VPP 4.8

Switch Frequency  
Default 1.2MHz  
Current Limit 4.8A.

Input Current= (2A\*2.5V)/5V/0.8=1.25A

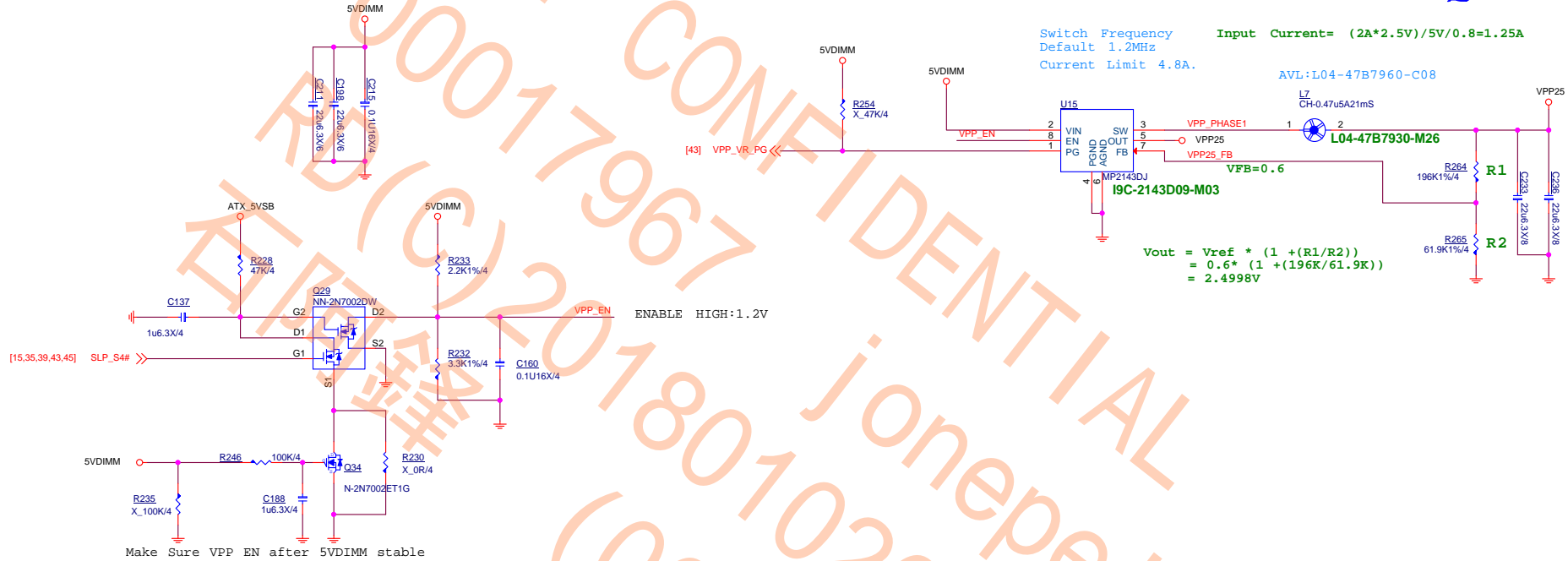
AVL:L04-47B7960-C08

LZ  
CH-0.47uA21mS

L04-47B7930-M26

VFB=0.6

$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.6 * (1 + (196K/61.9K)) \\ &= 2.4998V \end{aligned}$$

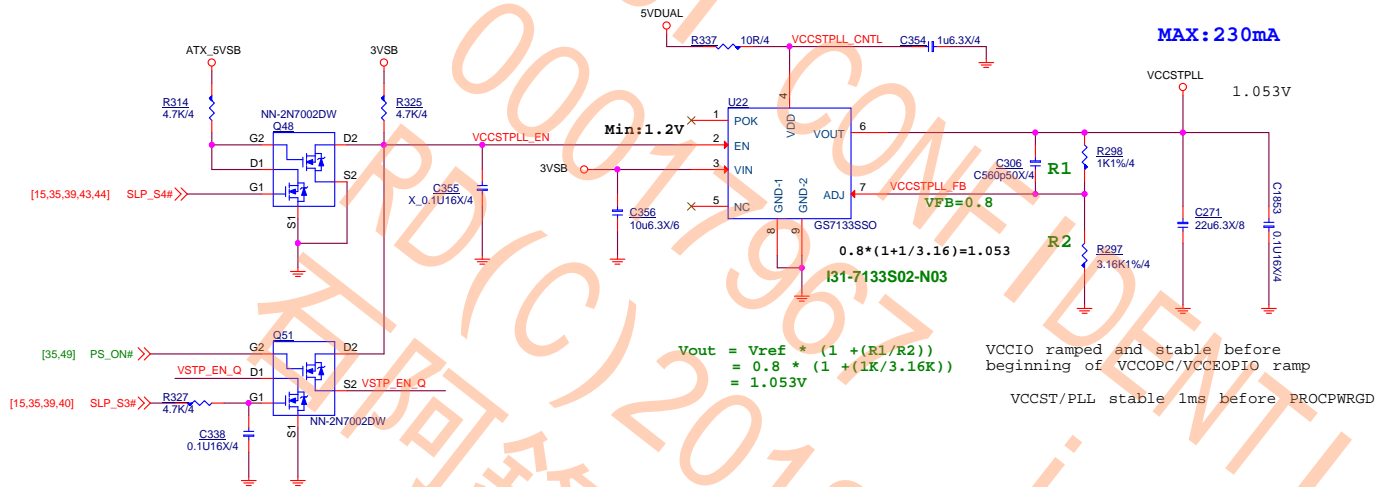


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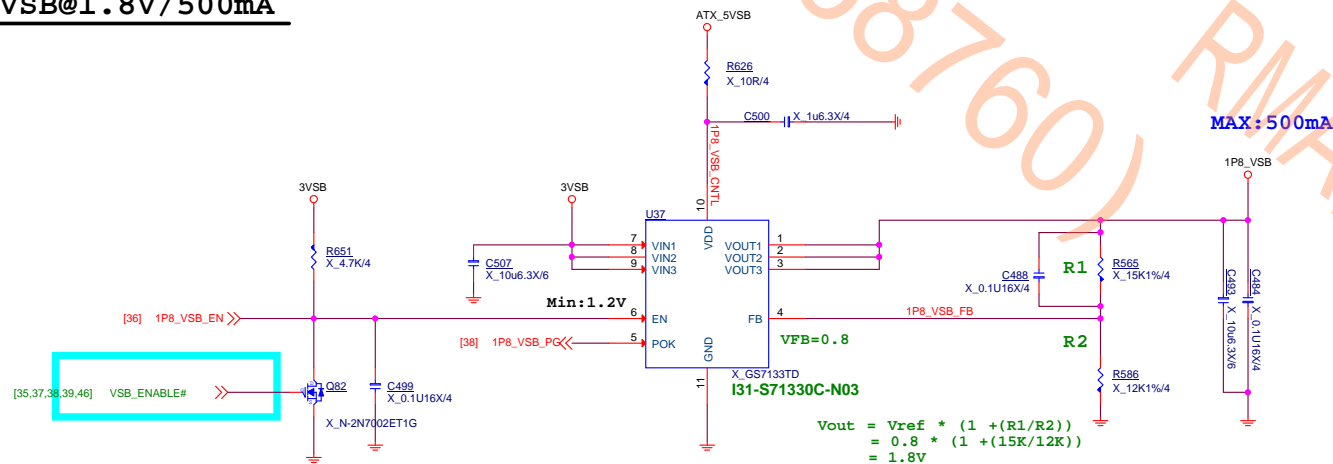
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Custom	DDR-MP2143-VPP25		10/2/30
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VCCSTPLL@1.05V/230mA



1P8\_VSB@1.8V/500mA



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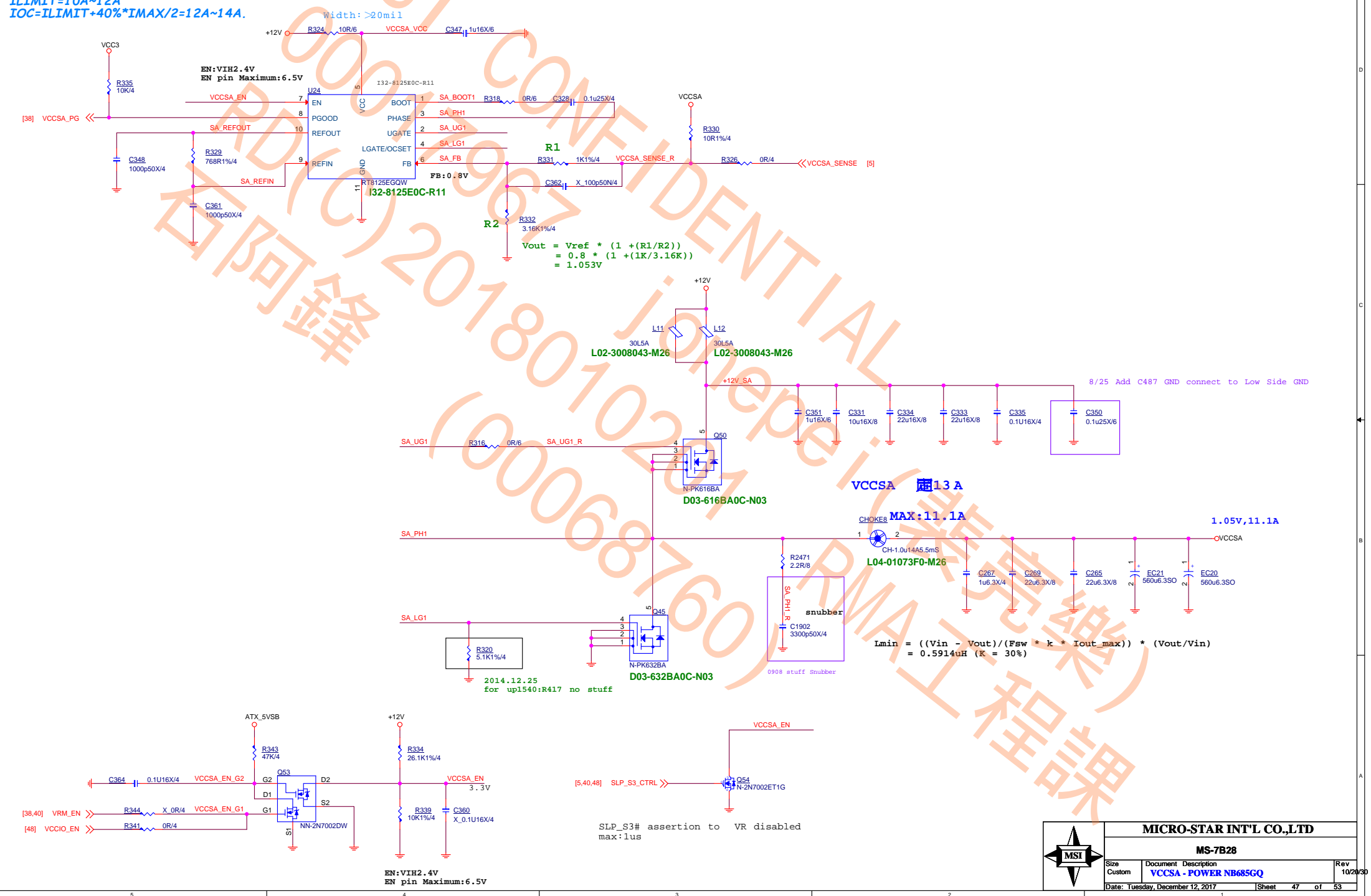
Size	Document	Description	Rev
Custom	CPU PWR ST/PLL		10/20/30
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Size Custom	Document Description <b>PCH Core power</b>	Rev 10/20/30
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VCCSA@1.05V/11.1A

IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.

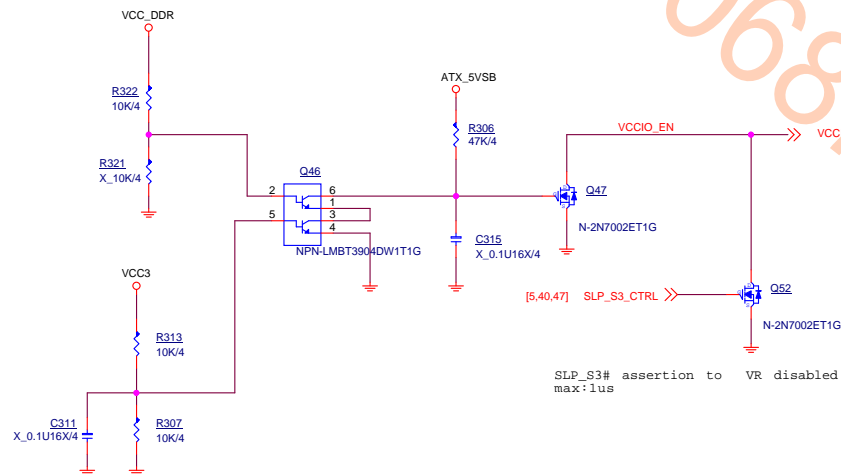
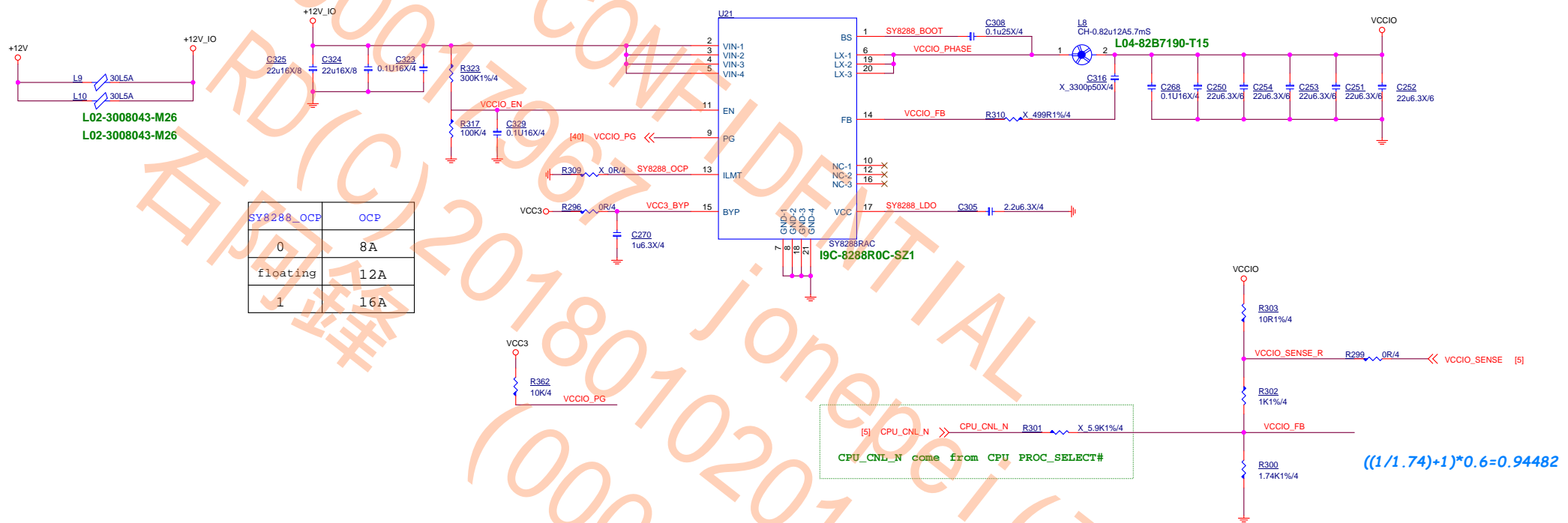


VCCIO@0.95V/6.4A

IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.

VCCIO 12A(floating

MAX:6.4A

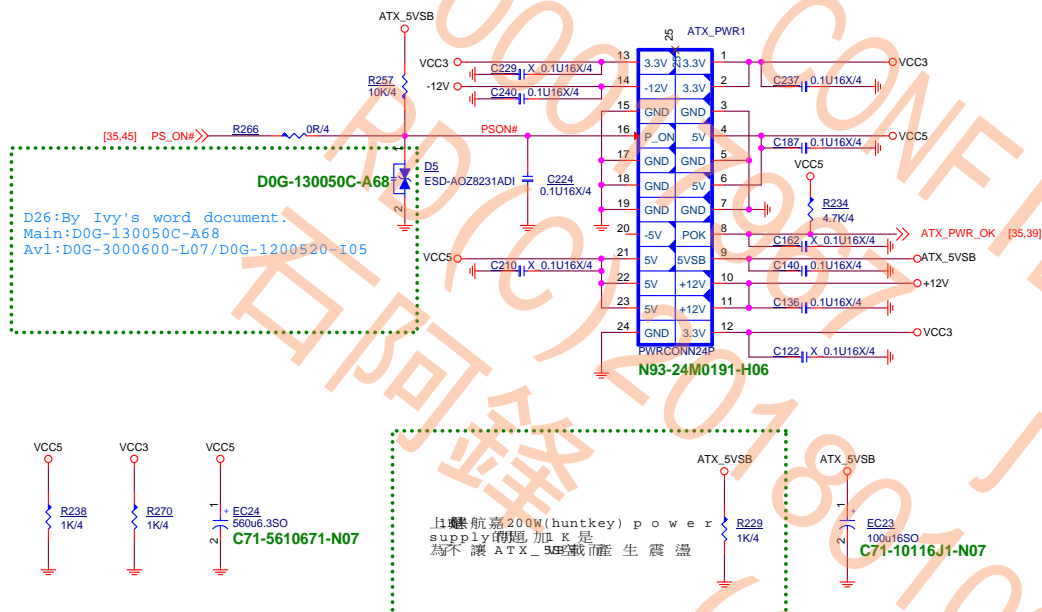


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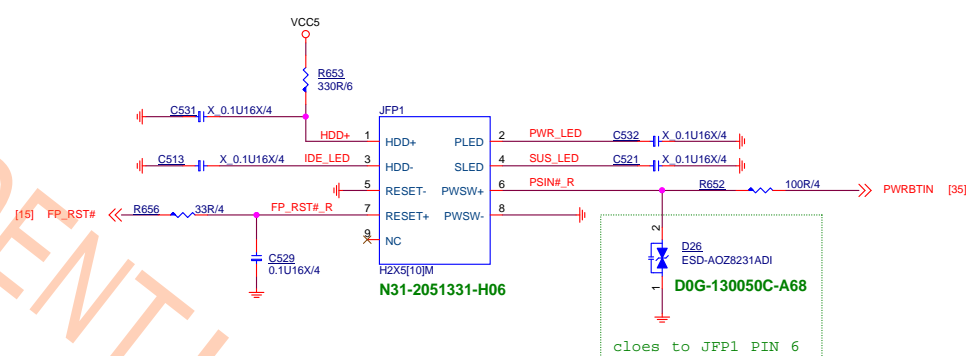
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Custom		VCCIO - POWER SY8288	10/2/30
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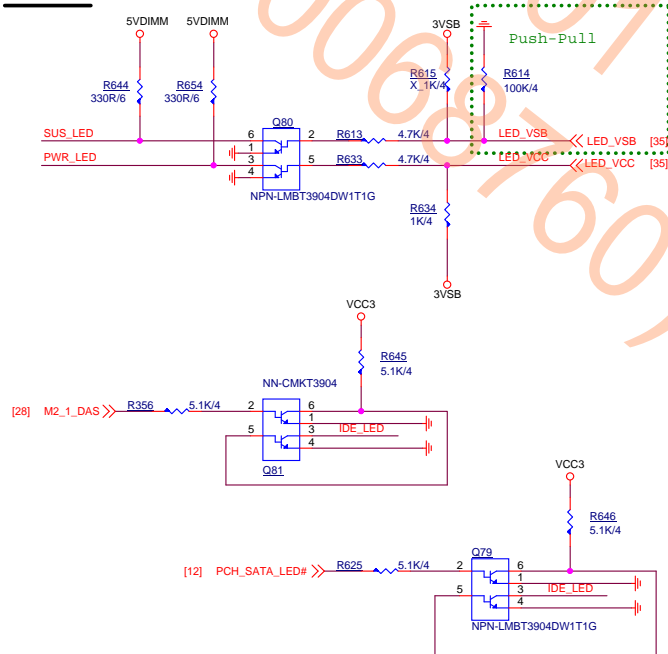
## ATX POWER CONNECTOR



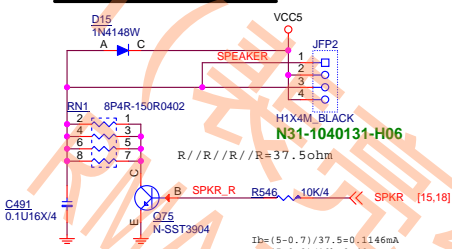
FRONT PANNEL



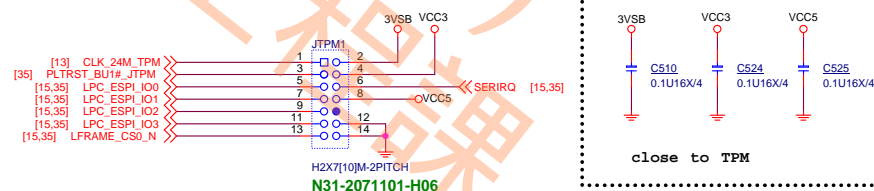
**LED**



### Speaker Pin Header



## TPM



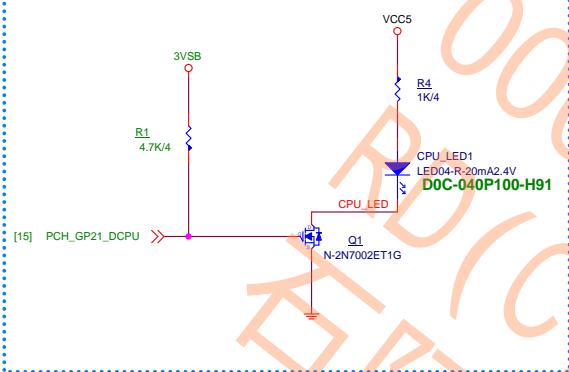
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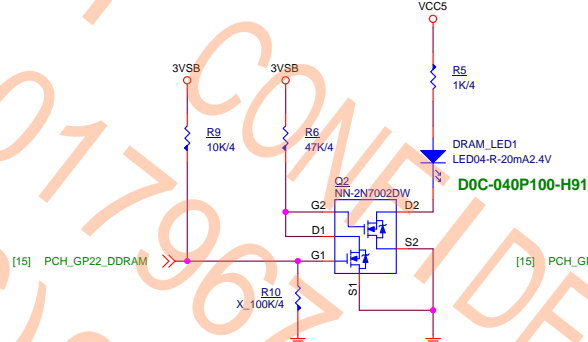
Size Custom	Document Description <b>ATX F_Panel/TPM/MSI_LED</b>	Rev 10/20/30
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## EZ DEBUG LED

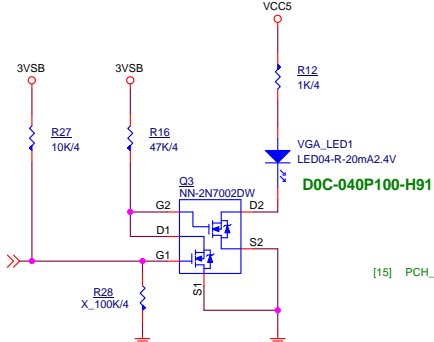
### CPU



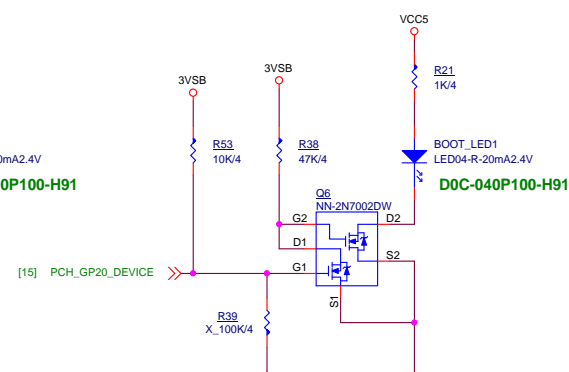
### DRAM



### VGA



### DEVICE



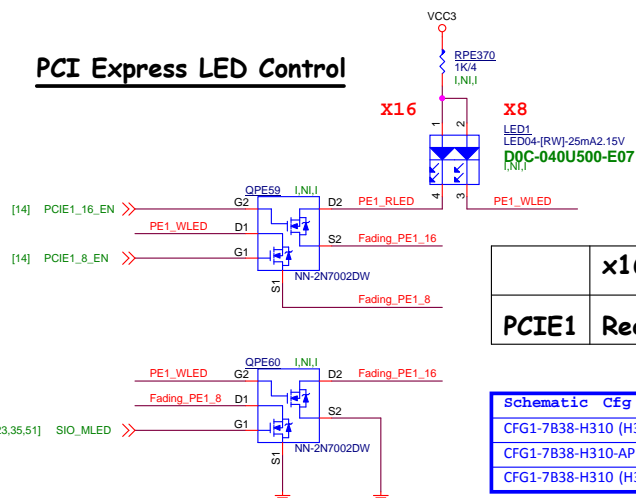
LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

### LED

RED:D0C-040P100-H91  
AVL:D0C-040S500-E07

WHI:D0C-040T200-H91  
AVL:D0C-040S200-E07

## PCI Express LED Control



	x16	x8
PCIE1	Red	White

Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V C

- 開機斷電狀態下，3個LED先維持 default 暗開機電後
1. 首先進行 CPU check CPU LED 亮，check PASS 後則 CPU LED 滅掉
  2. 接著依序進行 Memory / memory LED 亮 check PASS 後則 memory LED 滅掉
  3. VGA 的 check / VGA LED 亮，check PASS 後則 VGA LED 滅掉
  4. 因此最後正常順利開機後，三個 LED 都滅掉的。
- (系統重啟或其他原因造成系統重開機則重複上述流程)

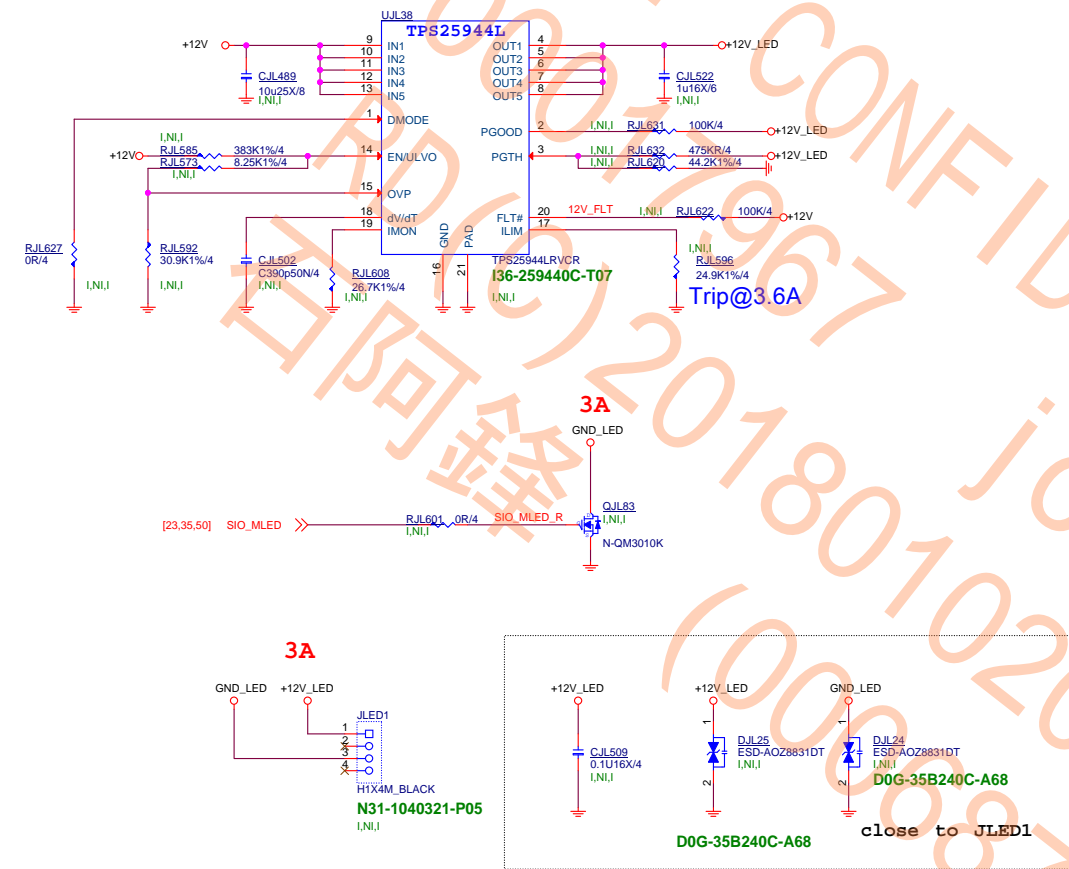


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LED Control by SIO(JLED1)



Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V C

OPTION BOM PARTS

Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	C

5010 Level

**A**

OPT EZ GPLUS  
LED04-R-20mA2-4V\_1608-HF  
D0C-040P100-H91  
Red

PD0-07B2810-E48  
PD0-07B2810-G37

OPT PCB GPLUS  
7B28\_10

**B**

OPT EZ PRO  
LED04-R-20mA2-4V\_1608-HF  
D0C-040T200-H91  
White

PK0-07B2820-E48  
PK0-07B2820-G37

OPT PCB PRO  
7B28\_20

**C**

OPT EZ GARCTIC  
LED04-R-20mA2-4V\_1608-HF  
D0C-040T200-H91  
White

PS0-07B2830-E48  
PS0-07B2830-G37

OPT PCB GARCTIC  
7B28\_30

5020 Level

**A**

OPT AUDLED GPLUS  
LED04-W-20mA3.25V  
USB\_C1\_24\_2  
D0C-040S600-E07  
Red

**B**

~~OPT AUDLED GPLUS  
LED04-W-20mA3.25V  
USB\_C1\_24\_2  
D0C-040S600-E07  
Red~~

**C**

OPT AUDLED GARCTIC  
LED04-W-20mA3.9V\_1608-RH  
USB\_C1\_24\_2  
D0C-040T300-H91  
White

60 Level

**A**

REAR U3  
OPT REARU3 GPLUS  
LANE\_U3  
USBAX2M\_RED-RH-2  
USB\_C1\_24\_2  
N53-18M0201-L06

DDR Slot  
OPT DDRSL0T GPLUS  
DDRIV\_288P\_RED-RH-1  
DDRIV\_D288  
N13-2880681-L06

PCIEx16 Slot  
OPT PCIEX16 GPLUS  
PCIEX16  
SLOT-PCI164P\_RED-2PITCH-RH-1  
N11-1641671-L06

DVI  
OPT VGA GPLUS  
VGA  
DVI24P\_BLACK-RH-17  
N5B-24F0771-EB6

VGA+DVI  
OPT VGA+DVI PRO  
VGA+DVI  
VGA\_DVI-RH-31  
N58-39F0371-EB6

PACK LABEL  
OPT LA GPLUS  
B310  
Label  
MKT  
G51-M1SPM62-Q13

**B**

REAR U3  
OPT REARU3 PRO  
LANE\_U3  
USBAX2M\_BLUE-RH-6  
USB\_C1\_24\_2  
N53-18M0091-F02

DDR Slot  
OPT DDRSL0T PRO  
DDRIV\_288P\_BLACK-RH-21  
DDRIV\_D288  
N13-2880561-L06

PCIEx16 Slot  
OPT PCIEX16 PRO  
PCIEX16  
SLOT-PCI164P\_BLACK-2PITCH-RH-38  
N11-1641221-L06

VGA+DVI  
OPT VGA+DVI PRO  
VGA+DVI  
VGA\_DVI-RH-31  
N58-39F0371-EB6

PACK LABEL  
OPT LA PRO  
B310  
Label  
MKT  
G51-M1SPM61-Q13

**C**

REAR U3  
OPT REARU3 GARCTIC  
LANE\_U3  
USBAX2M\_RED-RH-2  
USB\_C1\_24\_2  
N53-18M0201-L06

DDR Slot  
OPT DDRSL0T GARCTIC  
DDRIV\_288P\_BLACK-RH-21  
DDRIV\_D288  
N13-2880521-L06

PCIEx16 Slot  
OPT PCIEX16 GARCTIC  
PCIEX16  
SLOT-PCI164P\_WHITE-2PITCH-RH-4  
N11-1641601-L06

DVI  
OPT VGA GARCTIC  
VGA  
DVI24P\_BLACK-RH-17  
N5B-24F0771-EB6

VGA+DVI  
OPT VGA GARCTIC  
VGA  
DVI24P\_BLACK-RH-17  
N5B-24F0771-EB6

PACK LABEL  
OPT LA GARCTIC  
B310  
Label  
MKT  
G51-M1SPM60-Q13



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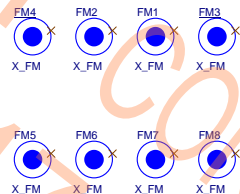
HS\_PCH1

PCH  
heatsink

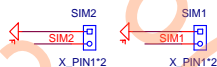
E31-0408580-K08  
HS-0408580

申請 中

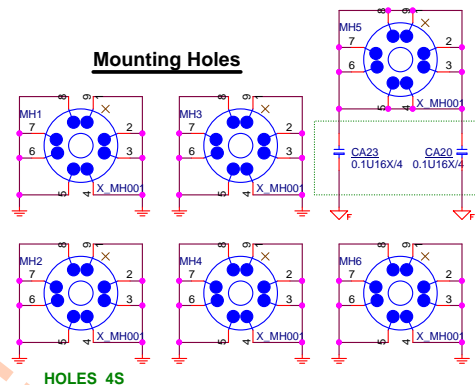
Optical Fiducial Marks-120



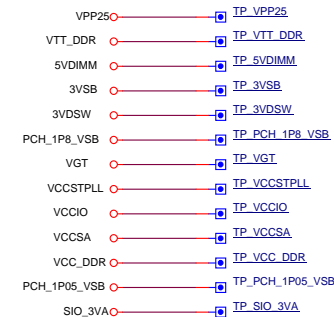
Simulation



Mounting Holes



HOLES\_4S



Near SIO CHIP



BAT1\_X1

BAT-BCR2032P

D06-0100101-K26

BIGS LA1

AMI

AMI

G51-M1SPXXA-A09

CPU\_H1

CPU  
鐵座

CPU\_H1

E21-7869020-F02

HDMI LA1

HDMI  
VIRTUAL

HDMI LABEL

Y01-RHDMI03-000

LA10

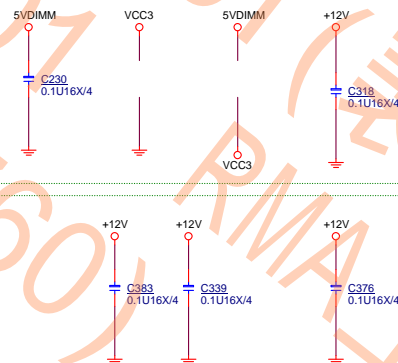
B310

SW

MKT

Y02-MU00170-CFO

return path



For M2 reference +12V USE  
please close to under M2



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